Performance of Aggressively Scaled Pseudomorphic HEMTs: A Monte Carlo Simulation Study

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The anticipated performance of pseudomorphic high electron mobility transistors has been extensively studied using Monte Carlo simulations when these devices are scaled into deep decanano dimensions. The scaling of devices with gate lengths of 120, 70, 50 and 30 nm has been performed in both lateral and vertical directions. The devices exhibit an improvement in transconductance during the scaling process, even though external resistances become a restrictive factor.

1. Introduction

A proper scaling of the conventional pseudomorphic high electron mobility transistors (pHEMT) can result in remarkable improvement of their performance [1]. For that reason, we have investigated the anticipated performance of a set of pHEMTs which have been scaled in both lateral and vertical direction with respect to the gate lengths of 120, 70, 50 and 30 nm. Our goal is quite realistic as suitable approaches (electron beam lithography, dry etching and δ-doping techniques) exist within III-V technology for controlling the critical atomistic limits. This is the first phase of a large experimental programme in Glasgow, aiming to establish Roadmap benchmarks for high-speed III-V devices. Today, this technology has been somewhat ahead of silicon in lithographic resolution and the engineering of active layers. However, with MOSFET approaching 0.1 μm [2] there are new incentives for exploring pHEMT scaling. Technologies based on a GaAs substrate reduce the cost and this type of substrate is still more manufacturable and has a large accessible scale of strain in comparison to an InP substrate.

2. Monte Carlo device simulator

The finite element Monte Carlo device simulator (MC/H2F) [3], with a judicious choice of parameters, enables us to study electron transport properties of pHEMTs and allows us to achieve I-V characteristics which are in very good agreement with experiment. MC/H2F is designed to use quadrilateral elements to depict the complex geometry of the pHEMTs and accurately calculates electrostatic effects caused by a shape of the gate and recess as well as surface potential pinning. The Monte Carlo module includes electron scattering with polar optical phonons; inter- and intra-valley optical phonons; non-polar optical and acoustic phonons and ionized and neutral

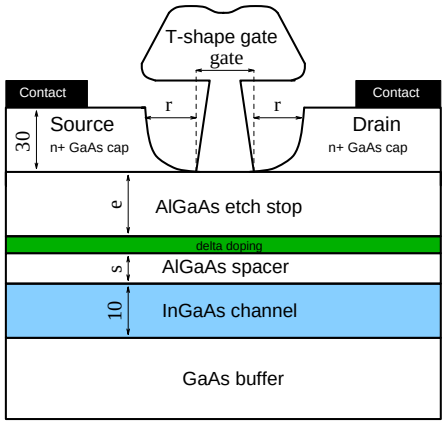

Figure 1: The cross-section of the simulated pHEMT.

impurities. In addition, alloy scattering and strain effects [4] are taken into account in the InGaAs channel. The non-parabolic energy dispersion relation is used for representing the band structure and calculating the scattering rates. To make our analytical band model of III-V material valid at high electric fields (up to 200-300 kV/cm), a form factor (the overlap integral) *G(E,E')* [5] has been employed for all scattering rates except for ionized impurities:

$$G(E, E') = \frac{(1 + \alpha E)(1 + \alpha' E') + \frac{1}{3}\alpha E \alpha' E'}{(1 + 2\alpha E)(1 + 2\alpha' E')}. \quad (1)$$

In equation (1), E is the initial electron energy, E' is the final electron energy after a scattering event, and α and α' are the non-parabolicity parameters for the electron in initial and final valleys, respectively. We implement Ridley's formulation [6] for ionized impurity scattering which allows for third-body exclusion during the collision of an electron with an ionized centre. We have used a direct technique to generate the final state of the electron after this type of scattering [7].

3. Effect of scaling on pHEMT performance

All scaling investigations are based on careful calibration of the MC device simulations against the 120-nm gate length pHEMT as designed and fabricated by the Nanoelectronics Research Centre at the University of Glasgow. The structure of the device is schematically drawn in Fig. 1. It has a T-shaped gate [8]; a 30-nm heavily Si-doped 2×10^{18} cm^{-3} n+ GaAs cap layer; an $Al_{0.3}Ga_{0.7}As$ etchstop layer; a 7×10^{12} cm^{-2} Si delta doped layer on top of an $Al_{0.3}Ga_{0.7}As$ spacer layer and, finally, an $In_xGa_{1-x}As$ channel with indium content x=0.2. The whole device structure is grown up on top of a 50-nm GaAs buffer.

Our device simulator MC/H2F is able to provide the I_D-V_D (drain current versus drain voltage) characteristics directly and thus represent the typical behaviour of the intrinsic device. To compare this with experimental data, it is necessary to include effect of the contact resistances of the source and drain in the I_D-V_D curves at a post-processing stage. The final I_D-V_D characteristics (open symbols in Fig. 2) for gate voltages from -0.6 V to 0.4 V are in good agreement with the experimental data (full symbols in Fig. 2). The external resistances of the source and drain, which have been used to remap the intrinsic I_D-V_D characteristics according

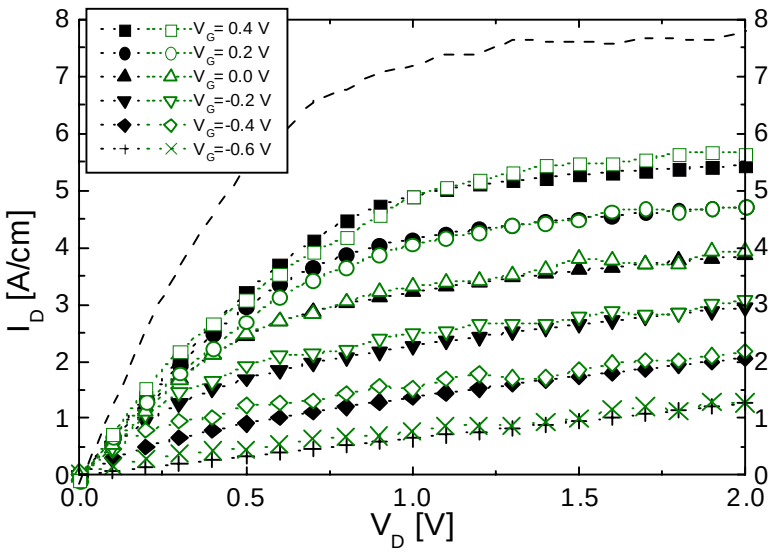

Figure 2: I-V characteristic of the calibrated pHEMT with a gate length of 120 nm. Full symbols are experimental data of the drain current versus the drain voltage for several fixed gate voltages. Open symbols represent a MC simulation when external resistances of the drain and source are included. The I-V characteristic for an intrinsic device (dashed line) is shown for comparison, for a gate voltage of 0.4 V.

Dimension of [nm]	Gate length [nm]			
	120	70	50	30
Recess (r)	50	29	21	13
Etchstop (e)	18	10	7	5
Spacer (s)	7	5	4	2

Table I: Dimensions used in the scaling process as referred to in Fig. 1.

the procedure described in Ref. 9, are 5.22 Ω and 0.6 Ω, respectively. The result for an intrinsic device is also shown for illustration by the dashed line for a gate voltage of 0.4 V only.

All lateral dimensions have been scaled proportionally to the respective gate length while, in the vertical dimension, the etchstop and spacer have been scaled with respect to technologically achievable dimensions. Thickness of the etchstop and space layers and the extent of the recess considered in the scaling process are given in Table I.

A rapid increase of the average channel velocity for the pHEMTs can be observed in Fig. 3 for gate lengths scaled from 120 nm to 70 nm despite the presence of a gate-edge fringing effect [10]. This improvement in channel velocity begins to saturate with the further scaling of the devices to 50 and to 30 nm. The continued device improvements in average channel velocity for sub-70 nm devices results solely from the reduction of the channel length. Although particles in this region can gain enough kinetic energy from high electric fields around the gate, they are slowed down by scattering with phonons (mainly by polar optical phonons and partially even by intervalley phonon transitions).

The drain current and transconductance are plotted in Fig. 4 as a function of gate voltage for intrinsic devices for a drain voltage of 1.5 V. The intrinsic transconductance increases steadily during the scaling process when the gate length is shrunk below 70 nm despite a small increase in the channel velocity. This means that with a proportional scaling from 120 nm to 30 nm (which includes the gate recess), the gate-fringing effect should have no significant influence on pHEMT performance. We should point out that when the device gate length decreases to deep decanano dimensions, it becomes comparable to the inelastic mean-free path of the carriers. Hence, electrons travelling through the gate region have a high probability of passing through this region without suffering any collisions. However, the reduction of the gate to channel separation below 10 nm may require inclusion of the effect of electron tunnelling between the gate and channel.

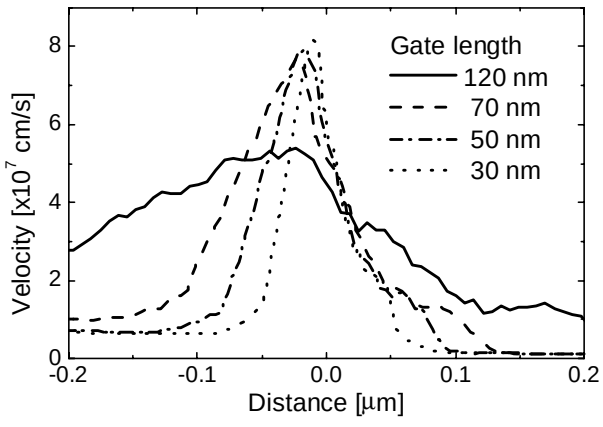

Figure 3: Average velocities along the InGaAs channel for a set of the scaled pHEMTs when drain and gate voltages are 1.5 V and 0.0 V, respectively

Fig. 5 illustrates the effect of the external contact resistances on the device performance, assuming that the value of these resistances remains unchanged in the scaling process. Influence of the external resistances on the device performance (on the drain current and the transconductance) becomes increasingly important with the reduction of the device dimensions. We expect that the problems related to the handling of external resistances will be one of the main issues for further technological improvement.

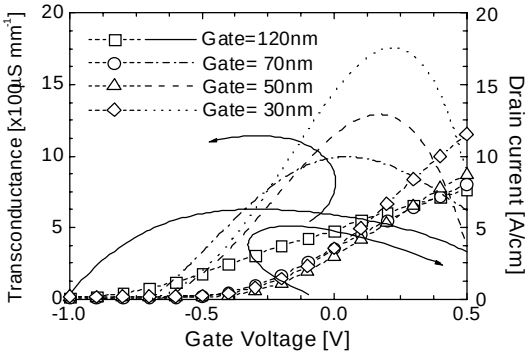

Figure 4: Transconductance and drain current versus the gate voltage for intrinsic devices of the scaled pHEMTs.

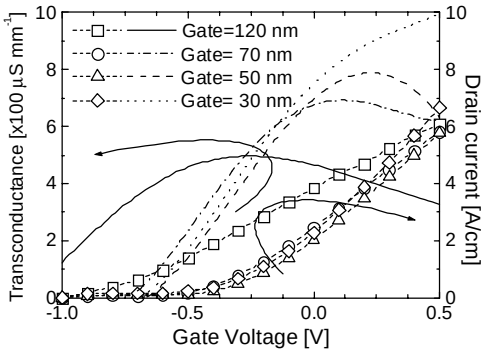

Figure 5: Transconductance and drain current versus the gate voltage for a set of the scaled pHEMTs when external resistances are include.

4. Conclusion

We have performed a Monte Carlo study of the pHEMTs' performance with low indium content when these devices are scaled into the deep decanano dimensions. We have not incorporated the phenomena of electron-electron (e-e) interactions into the Monte Carlo module. The e-e interactions are a fast process, responsible for the thermalization of electrons. Therefore, it should be considered only in regions with very high electron density. pHEMTs with the structure shown in Fig. 1 have two regions of high electron density: the heavily doped cap where changes in electron density have no influence on the drain current, and the delta-doped layer where the e-e interaction may reduce the induction of electrons into the channel. The latter is partially compensated for by considering a lower effective delta-doping concentration. Based on the careful calibration of the pHEMT with 120-nm gate length, we have found a continuous improvement in the intrinsic device performance with proportional scaling. If we wish to take advantage of the performance potential of the intrinsic device then contact resistances need to be reduced as much as possible.

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