Gate tunnelling and impact ionisation in sub 100 nm PHEMTs

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Abstract

Impact ionization and thermionic tunnelling as two possible breakdown mechanisms in scaled pseudomorphic high electron mobility transistors (PHEMTs) are investigated by Monte Carlo (MC) device simulations. Impact ionization is included in MC simulation as an additional scattering mechanism whereas thermionic tunnelling is treated in the WKB approximation during each time step in self-consistent MC simulation. Thermionic tunnelling starts at very low drain voltages but then quickly saturates. Therefore, it should not drastically affect the performance of scaled devices. Impact ionization threshold occurs at greater drain voltages which should assure a reasonable operation voltage scale for all scaled PHEMTs.

I Introduction

The performance of pseudomorphic high electron mobility transistors (PHEMTs) with gate lengths in sub-100 nm regime can be substantially enhanced when the devices are proportionally scaled in both lateral and vertical dimensions [1]. If only the lateral dimensions of the devices are scaled then the performance of PHEMTs with the sub-100 nm gate lengths deteriorates [1–3]. However, the constant-voltage scaling scenario imposed by circuit design requirements results in a very high fringing field [5] around the gate corners in the recess region. This high electric field and the associated impact ionisation can initiate early device breakdown [4]. A process which may supply carriers and facilitate impact ionisation in the normally depleted fringing field region around the drain end of the channel is the injection of electrons from the gate due to thermally assisted tunnelling [6] which results in a gate leakage current.

II Impact ionization and tunnelling

In this paper we study independently the impact ionisation and gate leakage current using Monte Carlo (MC) device simulations. We attempt to understand which of the above mechanisms dominates the breakdown of PHEMTs scaled with respect to gate lengths of 120, 90, 70, 50, and 30 nm. Our finite element Monte Carlo (MC) device simulator employs quadrilateral finite elements to depict the complex geometry around the T-shape gate and the both recesses of a PHEMT. The MC module involves electron scattering with polar optical phonons, inter- and intra-valley optical phonons, non-polar optical phonons and acoustic phonons, as well as ionized and neutral impurity scattering. The alloy potential scattering and strain effects on bandgaps, electron effective masses, phonon deformation potentials and energies are taken into account in the InGaAs channel. All scattering rates consider a form factor F (the overlap integral) given by [7]

$$F(E,E') = \frac{(1+\alpha E)(1+\alpha' E') + \frac{1}{3}\alpha E\,\alpha' E'}{(1+2\alpha E)(1+2\alpha' E')}, \qquad (1)$$

where an electron with the initial energy E has the final energy E' after a scattering. α and α' in the relation (1) are the non-parabolicity parameters for the electron in initial and final valleys respectively.

Impact ionisation is incorporated in the MC simulator as an additional scattering mechanism assuming that it starts at a threshold energy $E_{\rm th}$. The electron scattering rate due to impact ionisation then reads [8]

$$\Gamma(E) = P\ [(E-E_{\rm th})/E_{\rm th}]^A, \qquad (2)$$

where P and A are parameters which must be fitted to experimental data. Note here that the formula (2) is nothing more

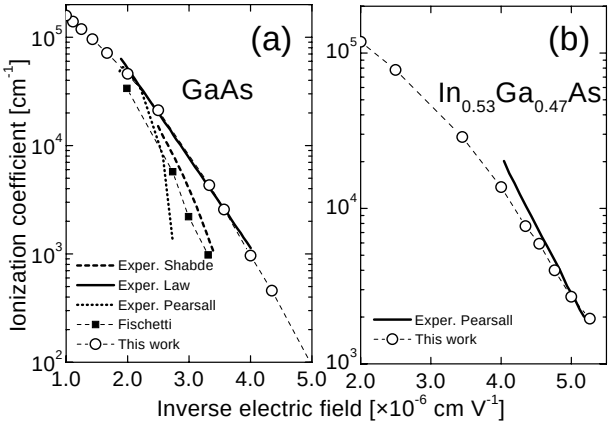

Figure 1: Impact ionisation coefficients versus inverse applied electric field obtained from simulations for GaAs (a) and for $In_{0.53}Ga_{0.47}GaAs$ (b) compared to experiments and full band simulations.

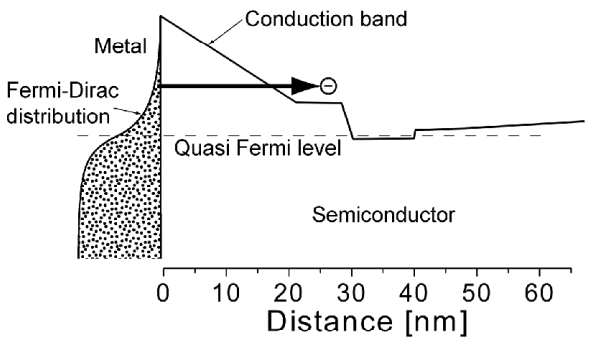

Figure 2: Cross section of the device through the middle of the gate at gate and drain biases of -1.0 and 2.0 V respectively. The simulation of tunnelling from the metal gate into the supply layer is schematically shown.

than a fitting expression based on Keldysh model for impact ionization. Such fitting expressions are often used in MC device simulations [9] due to the complexity of quantum mechanical approaches. We have used $A = 4$ for GaAs as it has been suggested in Ref. 8 and $A = 14$ for $In_{0.53}Ga_{0.47}As$ which is more difficult to simulate at a very high electric field.

Bulk simulations of the impact ionization coefficient on Fig.1 can satisfactorily reproduce measured data for GaAs and $In_{0.53}Ga_{0.47}As$ in the range of electric fields of interest. Since hole dynamics and the corresponding bipolar effects are not included in the MC simulations, the experimentally observed increase in the drain current at breakdown cannot be reproduced. Instead, we calculate an impact ionization assisted increase in the electron current of the devices. This allows us to define the

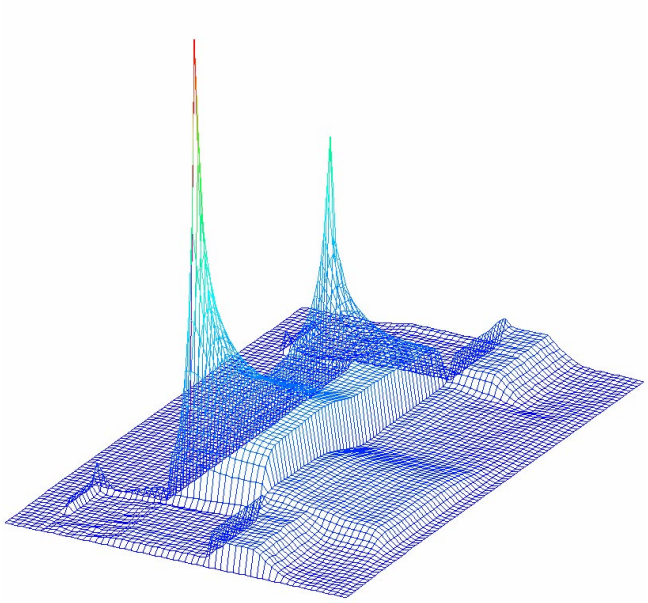

Figure 3: Electric field in the 120-nm gate length PHEMT at $V_G = -1.0$ V and $V_D = 2.0$ V. The huge electric fields which surround the gate and peak beneath the recesses determine a particle trajectory after tunnelling.

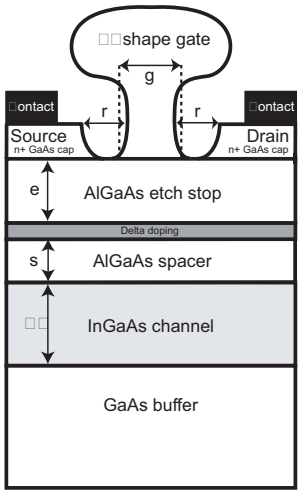

Figure 4: Cross section of PHEMT considered in this work. The distances referred to with a letter have been shrunk in the scaling process. The 10-nm InGaAs channel has an indium content of 0.2

bias conditions corresponding to the onset of impact ionization which is determined only by the electron dynamics.

Thermionic tunnelling is incorporated into the MC device simulator as an additional simulation procedure during each time step and proceeds as follows: a number of particles, which represent the electron density in the metal, is obtained after integration over the Fermi-Dirac distribution. Fig. 2 schematically illustrates the area of the Fermi-Dirac distribution from which the particle of a randomly selected energy E may tunnel into the device. In this way, the thermal broadening of electron distribution at room temperature is included into the tunnelling model. The tunnelling probability, T, is numerically calculated from the WKB approximation [10] by evaluating the integral

$$T(E) = \exp\{-2\frac{\sqrt{2m}}{\hbar}\int_0^w [V(x) - E]^{1/2}\, dx\}, \qquad (3)$$

where m is the electron effective mass in the device, w is the path along which the electron should tunnel through and $V(x)$ is the potential. This probability is used in a standard rejection technique to accept or reject the tunnelling event. If the tunnelling is accepted then the particle will be injected into the device at the energy E. The particle is injected in the direction of the strongest electric field (see Fig. 3). This process is repeated for each particle and at each mesh cell around the gate. The number of tunnelling particles is then used to calculate the gate tunnelling current.

III Impact ionisation and gate currents

The layout of a typical PHEMT under investigation is shown in Fig. 4. It has a T-shape gate; a 30 nm heavily doped (4×10^{18}cm^{-3}) n+ GaAs cap; an $Al_{0.3}$ $Ga_{0.7}As$ etchstop; a 7×10^{12}cm^{-2} Si delta doping; an $Al_{0.3}$ $Ga_{0.7}As$ spacer; and a 10 nm $In_{0.2}Ga_{0.8}As$ channel. The whole device structure is

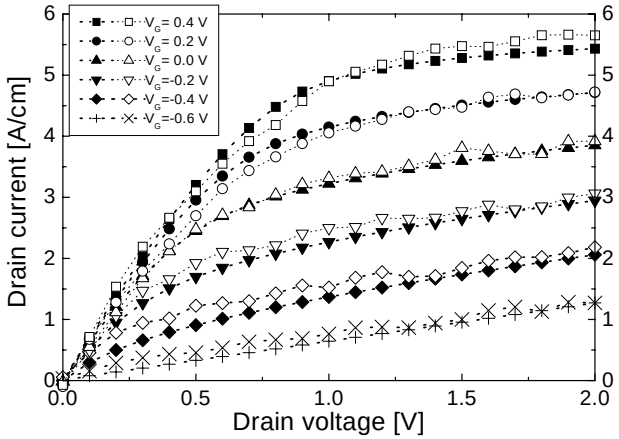

Figure 5: I_D-V_D characteristic of the PHEMT with a gate length of 120 nm. Full symbols represent experimental data for several fixed gate voltages. Open symbols are MC simulations when external resistances of the drain and source are included.

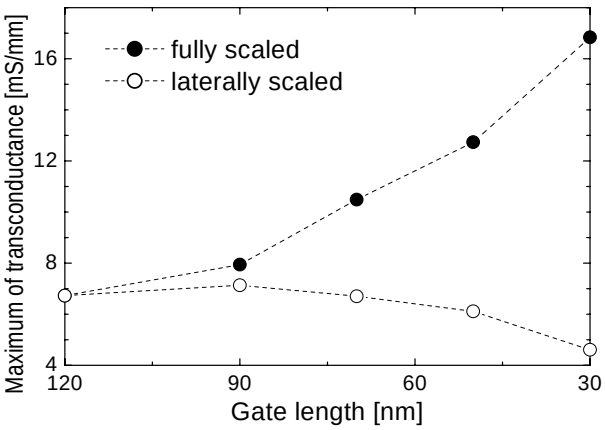

Figure 6: Maxima of transconductance as a function of the device gate lengths for fully scaled PHEMTs compared with those of laterally only scaled devices.

grown on top of a 50 nm thick GaAs buffer. The MC device simulator itself has been accurately calibrated against a real 120 nm PHEMT fabricated at the University of Glasgow [1] as shown on Fig. 5. The calibration requires the inclusion of contact resistances which are external to the MC simulation in order to compare the simulated I_D-V_D characteristics with experimental data. Fig. 6 compares the maxima of transconductance of the PHEMTs which are fully scaled in respect to the gate lengths of 90, 70, 50 and 30 nm with corresponding results obtained for laterally only scaled structures.

To find the corresponding threshold drain voltage for both breakdown mechanisms, the impact ionization and thermionic tunnelling assisted drain current is calculated from a number, N, of impacted or, respectively, tunnelled from the gate particles during the simulation time, t, as

$$I_D^{\text{assist}} = N\frac{e_S}{t}, \tag{4}$$

where e_S is the charge of a superparticle. A typical MC device simulation involves 50000 superparticles in the device and runs at least 10 ps with the time step of 0.2 ps (excluding the pre-simulation which has to establish a steady-state).

Fig. 7 shows the impact ionization assisted drain current as a function of the applied drain voltage at a very low gate bias. Impact ionization starts quickly increasing dramatically the drain current which leads eventually to complete device breakdown. The impact ionization events occur in the region of the fringing electric field below the recess at the drain side of the device (see Fig. 3). Electrons are extremely accelerated by a high electric field and may gain enough energy to overcome material bandgap. The impact ionisation event creates a new electron-hole pair. In this way a new electron is add to the transport process. However, the electron acceleration takes some time. As a result, the so-called dead space can be observed between the high electric field region and the actual place where an impact ionization event occurred.

In Fig. 8 the thermionic tunnelling assisted gate current is plotted, as a function of the drain voltage at the gate bias of

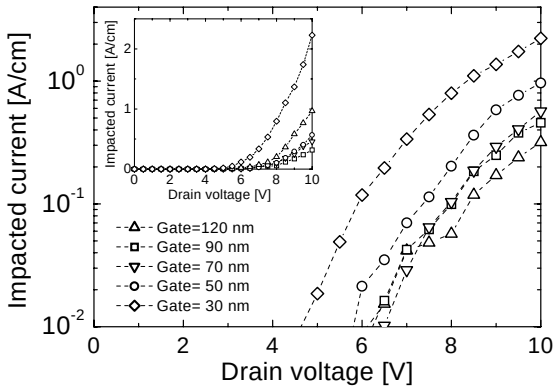

Figure 7: Impact ionisation assisted drain current versus the drain voltage at $V_G = -1.0$ V for the scaled PHEMTs. The inset shows the same curves on a linear scale.

-1.0 V. The drain current due to thermionic tunnelling has a different drain voltage dependence compared to the impact ionisation current on Fig. 7. It increases relatively sharply at lower drain voltages but then saturates at larger drain voltages [11]. The onset for both impact ionization and thermionic tunnelling decrease with device scaling. The thresholds for the impact ionization assisted drain current in Fig. 7 starts at much higher drain voltages compared to the thresholds of the gate tunnelling current. Fig. 8 also illustrates that although the thermionic tunnelling assisted gate current starts at a quite low drain voltage, it rapidly saturates at a large voltage even for the devices with a very small gate-to-channel separation. Therefore, all PHEMTs scaled below the 100 nm gate length will suffer from the increased gate current due to tunnelling. This additional current may negatively affect the improved device transconductance at very low gate biases in the scaling process. However, it still offers a practical operational range in device applications which are expected work at larger applied gate voltages. The indicated higher threshold voltages in Fig. 7 suggest that the breakdown caused by the impact ionisation is not of great concern for the scaling process.

Finally, the impact ionisation assisted drain current is shown

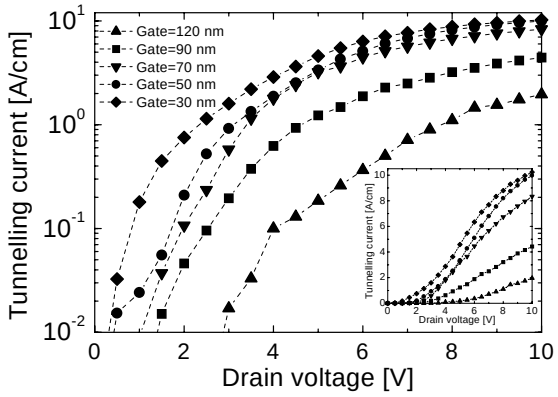

Figure 8: Tunnelling assisted drain current versus the drain voltage at $V_G = -1.0$ V for the scaled PHEMTs. The inset shows again the same curves on a linear scale.

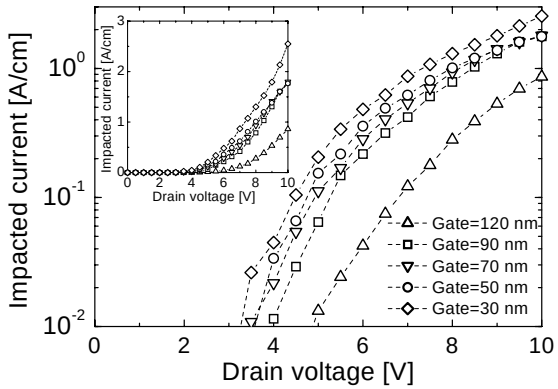

Figure 9: Impact ionisation assisted drain current versus the drain voltage at $V_G = -1.0$ V for the scaled PHEMTs when the tunnelling is included in the device simulations. The inset shows again the same curves on a linear scale.

in Fig. 9 for the scaled PHEMTs when the thermionic tunnelling is involved as well in the device simulations. The impact ionisation occurs at lower drain voltages in all scaled devices when compared to Fig. 7 because the tunnelling provides many additional energetic carriers for the device transport. The impact ionization threshold voltage lowers from 6.2 V to 5 V for the 120 nm PHEMT and from 4.7 V to 3.2 V for the 30 nm device. Also, overall amount of the impacted current is slightly higher when compared to the simulations with the excluded tunnelling from the gate.

IV Conclusions

We have studied two breakdown mechanisms in scaled PHEMTs, impact ionization and gate thermionic tunnelling. This study has been carried out using our MC device simulator MC/H2F. Impact ionization has been incorporated into the device simulator as an additional scattering mechanism whereas thermionic tunnelling has been treated as an additional simulation process at each time step. The number of particles created by these two processes allow us to calculate the impact ionization assisted drain current and the gate tunnelling current. The thresholds of both phenomena decrease with proportional scaling from gate length of 120 to 90, 70, 50, and 30 nm. The gate tunnelling current starts at quite low drain voltages and then saturates at large drain voltages. Gate leakage may negatively impact the performance of scaled devices having gate lengths less than 100 nm. The impact ionization assisted drain current begins at much higher threshold voltages even for the 30 nm gate length PHEMT. These relatively large threshold voltages indicate that impact ionization is not a matter of great concern for the anticipated device operational range. However, at low gate voltages, the gate leakage current due to thermionic tunnelling dominates device breakdown, also leading to an excessive leakage in aggressivelly scaled devices at supply voltages above 2 V. Therefore, one crucial task in PHEMT scaling to sub-100 nm dimensions is the elimination of gate tunnelling by, for example, using high K dielectrics.

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