Available online at www.sciencedirect.com
SCIENCE DIRECT®
Solid-State Electronics 48 (2004) 1223–1232
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Role of multiple delta doping in PHEMTs scaled to sub-100 nm dimensions

K. Kalna *, A. Asenov

Device Modelling Group, Department of Electronics & Electrical Engineering, Rankine Building, Oakfield Avenue, University of Glasgow, Glasgow G12 8LT, Scotland, UK

Received 1 October 2003; received in revised form 1 December 2003; accepted 1 February 2004

The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

Scaling of pseudomorphic high electron mobility transistors (PHEMTs) into deep sub-100 nm dimensions can dramatically improve their performance. However, the reduction in the channel carrier density of the scaled devices with a single delta doped layer (DDL) has a detrimental effect on the drain current and consequently on the power handling capability. The linearity of the scaled transistors also deteriorates. These negative aspects of the scaling can be compensated with an additional DDL introduced into the device structure. We employ Monte Carlo device simulations to study the effect of two possible placements of the second DDL on the performance of aggressively scaled PHEMTs. The placement of the second DDL below the channel increases the drive current and linearity but does not improve the transconductance. The placement of the second DDL above the original one increases the current and improves the transconductance by up to approximately 45% but does not improve linearity. In order to understand the breakdown limitations of the scaled devices both the impact ionization and the gate tunnelling currents are included in the Monte Carlo simulator and monitored in the simulations.

Keywords: Pseudomorphic HEMT; Scaling; Monte Carlo simulation; Double delta doping; Transconductance

1. Introduction

InP based HEMTs with channel lengths below 30 nm and cut-off frequencies above 500 GHz have already been demonstrated experimentally [1–3]. Recent simulation studies [4,5] have also shown that the performance of conventional pseudomorphic high electron mobility transistors (PHEMTs) with low In content in the channel fabricated on GaAs substrates can be substantially improved when these devices are proportionally scaled down to sub-100 nm dimensions in both lateral and vertical directions. The PHEMTs scaled only in the lateral dimensions exhibit a deterioration in device performance [4,6,7]. However, for transistors with a single delta doped layer (DDL), the reduction of the gate-to-channel separation in the proportional scaling and the constrained doping efficiency reduces the carrier density in the channel. This decrease has a detrimental effect on the drive current as well as the device linearity [4]. The decrease in the drive current can be compensated with additional DDL introduced into the device structure [8] in order to create a double delta doped PHEMT.

The second DDL can be placed either below the channel to achieve a better device linearity [9,10] or above the original DDL, near the gate, to improve the device transconductance [11]. Using self-consistent ensemble Monte Carlo (MC) simulations we systematically examine the impact of these two possible placements on the performance of scaled PHEMTs. The

* Corresponding author. Tel.: +44-141-330-4792; fax: +44-141-330-4907.
E-mail address: kalna@elec.gla.ac.uk (K. Kalna).

0038-1101/$ - see front matter © 2004 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2004.02.008

PHEMTs are considered to be proportionally scaled down from a 120 nm gate length to 70, 50 and 30 nm, respectively.

Due to increased electric fields and reduced gate-to-channel separation scaled PHEMTs are likely to suffer from early breakdown symptoms. Therefore, mechanisms leading to device breakdown are examined in this work in order to estimate the operating voltage range. We have included in our simulations impact ionization [12,13] which may occur due to the increased electric fields and thermionic tunnelling [14,15] from the gate which may occur due to the reduced gate-to-channel separation in the scaling process. The excess drain current produced by impact ionization or gate tunnelling has been calculated as a function of the applied bias to find thresholds for both these mechanisms.

The investigations have been performed using a MC device simulator the salient features for which are described in Section 2. The *I–V* characteristics and the device transconductances for both double-doped designs of PHEMTs are presented in Section 3. Section 4 is devoted to device breakdown mechanisms including impact ionization and gate tunnelling. Conclusions make up Section 5.

2. The Monte Carlo device simulator

The whole study has been carried out using the MC device simulator MC/H2F [4,16]. The MC module includes electron scattering with polar optical phonons; inter- and intra-valley nonpolar optical phonons; acoustic phonons and ionized and neutral impurity scattering. Alloy scattering and strain effects are also taken into account in the InGaAs channel. An extended analytical band structure model of materials in this MC module allows for the accurate description of electron transport up to an electric field of 400 kV/cm [4]. The finite element discretisation used in MC/H2F accurately handles the complex geometry of the PHEMT, particularly around the gate and recesses [17].

For the purpose of this study the MC simulator has been enhanced with appropriate impact ionization and gate tunnelling models. Impact ionization is included as an additional scattering mechanism into the MC module. Assuming that impact ionization starts at a threshold energy E_{th} the corresponding electron scattering rate can be expressed as [18,19]

$$\Gamma(E) = \mathscr{P}(E - E_{\text{th}})^{\mathscr{A}}, \tag{1}$$

where $\mathscr{P}$ and $\mathscr{A}$ are parameters which must be fitted to experimental data and/or to the calculated electron scattering rates using full band models and matrix elements in the Born approximation [19]. The expression (1) is suitable for GaAs and AlGaAs because they are quite wide bandgap materials with a hard impact ionization threshold [19]. However, in the case of InGaAs, a different type of exponential expression has to be employed to correctly reproduce the impact ionization scattering rate. This is due to the fact that InGaAs has a narrower bandgap and a much softer impact ionization threshold [20]. For this material we have adopted the expression from [20] which reads

$$\Gamma(E) = \mathscr{P}\exp[\mathscr{A}(E - E_{\text{th}})]. \tag{2}$$

Such fitting expressions are often used in MC device simulations [21,22] due to the complexity of the full quantum mechanical approach. The bulk MC simulations of the impact ionization coefficient as a function of the inverse electric field, plotted in Fig. 1, reproduces quite accurately the experimental data for GaAs using the fitting expression (1) as well as the experimental data for $In_{0.53}Ga_{0.47}As$ when the exponential fitting expression (2) is employed. The fitting parameters $\mathscr{P}$ and $\mathscr{A}$ as well as threshold energies for both GaAs and $In_{0.53}Ga_{0.47}As$ are summarised in Table 1. Note that to reproduce a behaviour of the impact ionization coefficient in $In_{0.53}Ga_{0.47}As$ with the power fitting expression (1) is extremely difficult [29].

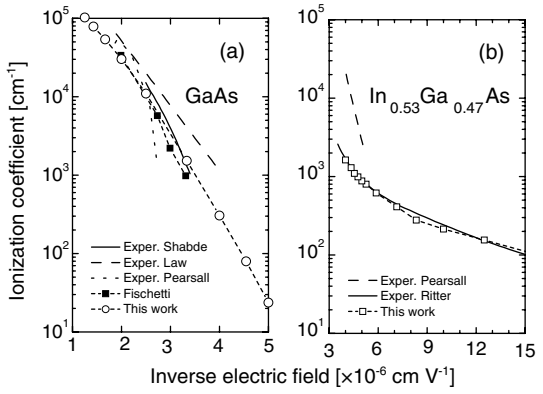

Fig. 1. Impact ionization coefficients versus inverse applied electric field obtained from MC simulations for GaAs (a) and for $In_{0.53}Ga_{0.47}As$ (b). Experimental data [23–25] and full band MC simulations [26] for GaAs and experimental data [27,28] for $In_{0.53}Ga_{0.47}As$ are also plotted.

Table 1
Parameters $\mathscr{P}$ and $\mathscr{A}$ used to calculate the impact ionization rates using formulae (1) and (2), and threshold energies for GaAs and $In_{0.53}Ga_{0.47}As$, respectively

Parameter	GaAs	$In_{0.53}Al_{0.47}As$
$\mathscr{P}$	1.4×10^{11}	4.5×10^{8}
$\mathscr{A}$	5.2	2.7
E_{th} [eV]	1.89	0.753

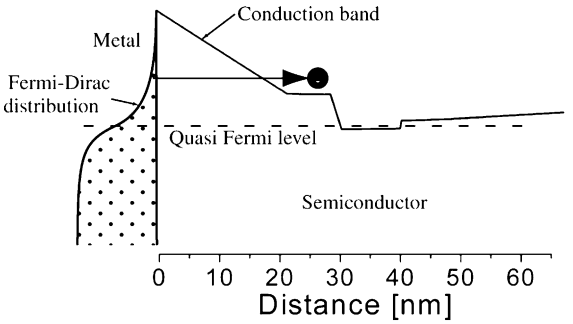

Fig. 2. Cross section of PHEMT through the middle of the gate with gate and drain biases of −1.0 and 2.0 V, respectively. A particle tunnelling from the metal gate into the supply layer is schematically shown.

When impact ionization scattering is selected in the MC device simulation, a new particle is created with the energy which satisfies the energy conservation requirements in the process. The momentum of the new particle is determined using the random-**k** approximation which has been shown to be valid for both GaAs and $In_{0.53}Ga_{0.47}As$ [30]. The position of the new electron is then randomly chosen within the mesh cell where the impact ionization event has taken place.

Thermionic tunnelling from the gate is incorporated in MC/H2F as an additional simulation procedure. During each time step the number of particles (which represent the electron density in the gate metal) is obtained after integration over the Fermi–Dirac distribution. Fig. 2 schematically illustrates the area of the Fermi–Dirac distribution used to randomly select a particle with energy E which may tunnel into the device. In this way, the thermal broadening of electron distribution at room temperature is included into the tunnelling model. The tunnelling probability, T, for such a particle is numerically calculated from the WKB approximation [31] by evaluating the integral

$$T(E) = \exp\left\{ -2\frac{\sqrt{2m}}{\hbar}\int_0^w [V(x) - E]^{1/2}\,\mathrm{d}x \right\}, \qquad (3)$$

where m is the electron effective mass in the device, w is the path along which the electron should tunnel through and $V(x)$ is the potential obtained by solving the Poisson equation during the simulation run. This probability is used in a standard rejection technique to accept or reject the tunnelling event. If the tunnelling is accepted then the particle will be injected into the device with energy E in the direction of the strongest electric field. This process is repeated for each particle in the gate metal and at each mesh cell around the gate. The number of tunnelling particles is then used to calculate the gate tunnelling current.

The WKB approximation works very well in this case since the gate tunnelling occurs at the metal–semiconductor interface [32]. This situation is somehow different from the gate tunnelling in silicon MOSFETs where for the insulator–semiconductor interface the WKB approximation tends to overestimate the tunnelling [33].

3. Double delta doped PHEMTs

The PHEMTs under investigation, illustrated in Fig. 3, have a symmetrical single recessed T-gate [17]. The

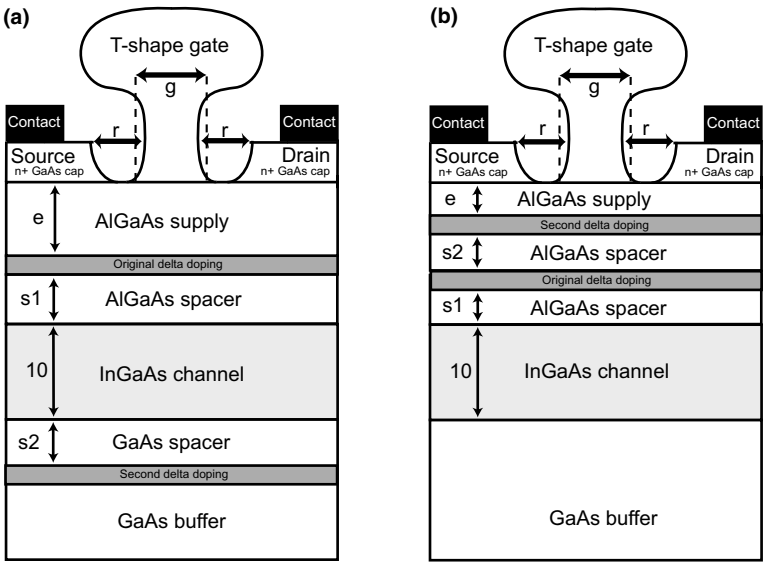

Fig. 3. A schematic view of a device with two positions of additional doping: (a) The second DDL is below the channel or (b) the second DDL is above the original doping layer, near to the gate.

vertical layer structure includes a heavily doped (4×10^{18} cm^{-3}), 30 nm GaAs cap layer, and an $Al_{0.3}Ga_{0.7}As$ Schottky 'supply' layer. The first Si DDL is separated by an $Al_{0.3}Ga_{0.7}As$ spacer from an InGaAs channel which is made of a low indium content of 0.2. The simulated PHEMTs are proportionally scaled in both lateral and vertical dimensions from a gate length of 120 to 70, 50, and 30 nm [4]. The gate recess width r (see Fig. 3) and layer thicknesses of the scaled devices are specified in Table 2. The additional DDL, separated by a GaAs spacer, can be placed either below the channel as illustrated by Fig. 3(a), or alternatively above the original DDL, near the gate, as shown in Fig. 3(b). Although the typical deposited concentration of the standard DDL is intended to be 7×10^{12} cm^{-2} due to limited doping efficiency only half of the concentration, i.e. 3.5×10^{12} cm^{-2}, is active in a fabricated device. The placement and concentration of the additional DDL is always chosen to avoid a creation of the parasitic channel and to have a good modulation efficiency [34]. Further optimisation of the second DDL position and concentration is a subject of this investigation.

The MC device simulator has been accurately calibrated against a real single doped 120 nm PHEMT fabricated at the University of Glasgow [4]. The calibration has been performed by comparing the calculated and measured I_D–V_G characteristics at low (0.1 V) and high (2.0 V) drain voltages and families of I_D–V_D characteristics for fixed gate voltages [4]. Note that the inclusion of contact resistances not present in the MC simulations, is required for the proper comparison between measurements and simulations [35,36]. For the measured 120 nm PHEMT the overall external resistance of the source and drain obtained experimentally was 5.22 Ω [4]. The excellent agreement illustrated in Fig. 4 is a starting point of our investigation.

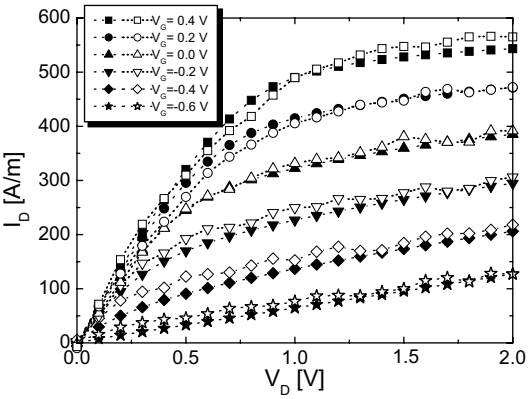

Fig. 4. I_D–V_D characteristic of the PHEMT with a gate length of 120 nm. Full symbols represent experimental data for several fixed gate voltages. Open symbols are MC simulations when contact resistances (5.22 Ω) of the drain and source are included.

The conduction band profiles of 120 nm double-doped PHEMTs with the second DDL placed either below or above the channel are shown in Fig. 5(a) and (b), respectively at $V_G = 0.0$ V for three different effective doping concentrations. It is clear that the channel carrier densities in the double-doped structures are much higher compared to the single-doped one. For example, when a second DDL with a doping concentration of 1.0×10^{12} cm^{-2} is placed behind the channel, the channel carrier sheet density increases from 2.078×10^{12} cm^{-2} in the single doped 120 nm PHEMT to 2.778×10^{12} cm^{-2} in the double-doped structure. The equivalent increase is even higher for the 70 nm device where the carrier sheet density rises from 1.686×10^{12} cm^{-2} to 2.401×10^{12} cm^{-2} in the double-doped device. Note that the carrier sheet

Table 2
Widths of layers and recesses in the set of scaled double-doped PHEMTs

The second DDL behind the channel				
Recess width, r [nm]	50	29	21	13
Gate length, g [nm]	120	70	50	30
Supply layer, e [nm]	18.5	10	7	5
First spacer layer, $s1$ [nm]	7	5	4	2
Channel layer [nm]	10	10	10	10
Second spacer layer, $s2$ [nm]	4	4	4	4
The second DDL above the original DDL				
Recess width, r [nm]	50	29	21	13
Gate length, g [nm]	120	70	50	30
Supply layer, e [nm]	9.5	6.5	5	3
First spacer layer, $s1$ [nm]	8.5	4.5	3.5	2
Second spacer layer, $s2$ [nm]	7	3.5	2.5	1.5
Channel layer [nm]	10	10	10	10

The upper table summarise the widths of the double-doped design with the second DDL behind the channel while the lower table contains the layer widths for the double-doped PHEMTs with the second DDL above the original doping layer.

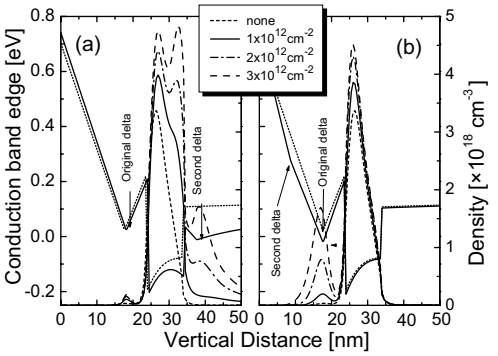

Fig. 5. The conduction band profile and carrier density as functions of the depth in the 120 nm double-doped PHEMTs with (a) an additional layer below the channel or (b) above the original doping layer for its various doping concentration. The conduction band in the single-doped PHEMT is shown by dot lines while the full lines are the conduction bands in the respective double-doped PHEMTs. The Fermi energy is set to zero.

density of the single-doped structure calculated from the self-consistent Poisson–Schrödinger solution has been precisely calibrated against the measured density in material grown and used in the fabrication of the referenced 120 nm PHEMT.

The I_D–V_G characteristics and transconductances of single- and double-doped PHEMTs with gate lengths of the 120 and 70 nm at a fixed drain voltage of 1.5 V are compared in Figs. 6 and 8, respectively. Results are presented for three different concentrations of the additional DDL placed behind the channel and separated with a 4 nm spacer. The current in the double delta doped PHEMTs continuously increases with increasing delta doping concentration of the second delta layer. Figs. 6 and 8 also show that when the additional doping

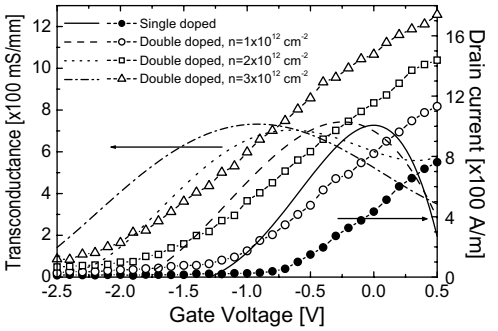

Fig. 6. Intrinsic I_D–V_G characteristics (symbols) and transconductances (lines) for the 120 nm gate length PHEMTs at $V_D = 1.5$ V. The double-doped PHEMTs with the second DDL placed below the channel are compared to the single-doped device.

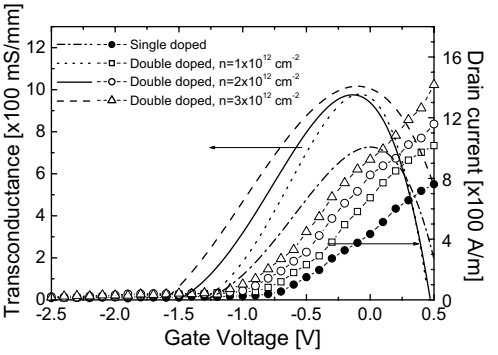

Fig. 7. Intrinsic I_D–V_G characteristics (symbols) and transconductances (lines) for the 120 nm gate length PHEMTs, again at $V_D = 1.5$ V, when the second DDL is placed above the original DDL.

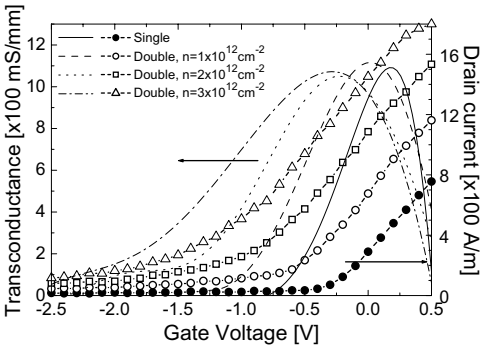

Fig. 8. Intrinsic I_D–V_G characteristics (symbols) and transconductances (lines) for the 70 nm gate length device at $V_D = 1.5$ V. The double-doped PHEMT has the second delta doping placed below the channel.

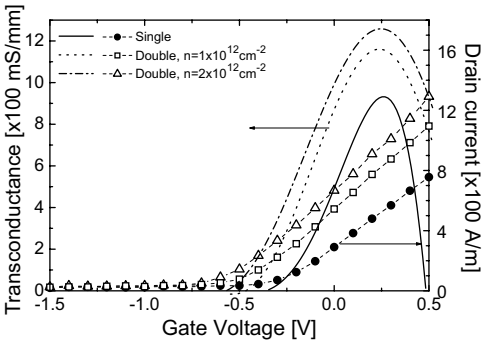

Fig. 9. Intrinsic I_D–V_G characteristics (symbols) and transconductances (lines) for the 70 nm PHEMTs at $V_D = 1.5$ V. The double-doped PHEMT with the second DDL placed above the original DDL is compared with the single-doped design.

layer is placed below the channel, the transconductance peak broadens resulting in the improved linearity of the

device, although its maximum transconductance remains close to that of the single-doped structure. Figs. 7 and 9 summarise the simulation results for the 120 and 70 nm devices with the second delta doping above the channel, near to the gate. The spacer between the first and the second DDL in this case is 8.5 and 4.5 nm, respectively.

If the second DDL is placed below the device channel the efficiency of the gate control over the channel transport is not changed remaining the same as in the single-doped devices. In the same time the carrier density in the channel is substantially increased which results in the larger drive current an in excellent device linearity. The effect of placing the second DDL above the original one is rather different. The increase in the current shown in Figs. 7 and 9 is not as large as in those devices with the delta doping below the channel but the maximum transconductances are much larger (about 45% for the 120 nm, 40% for the 70 nm) than the maximum transconductance of the single-doped PHEMT. The second DDL placement above the channel, close to the gate, is very beneficial for the gate control over the channel keeping the carriers close to the top interface. It screens electric fringing fields around the gate reducing the effective channel length and allowing carriers to pass more quickly through the gate region compared with a single-doped PHEMTs. Therefore, ballisticity of carriers in the channel of double delta doped PHEMTs with the second DDL above the original one is higher than those in the single-doped device and in the double doped with the second DDL below the channel. The placement of the second DDL above the channel is also beneficial for the access resistances of the channel which are lowered considerably [37]. Therefore, the better gate control, improved ballistic transport and lower access resistances all together contribute to the higher transconductance of the PHEMTs with the additional DDL placed above the original delta doping.

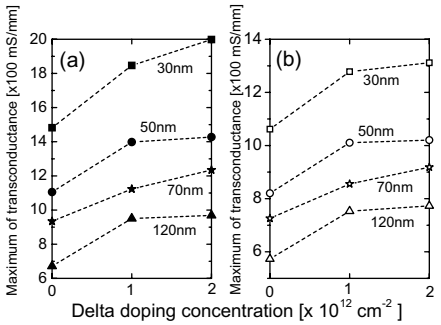

Fig. 10. Maxima of transconductances versus the second delta doping concentration for (a) an intrinsic device and (b) with external resistances included. The respective gate lengths are also indicated. Zero second delta doping concentration represents a single-doped PHEMT.

The improvement in the maximum intrinsic transconductance as a function of the sheet concentration of the second DDL placed above the first is illustrated in Fig. 10 for the complete set of the scaled devices. Increasing the concentration of the second delta doping above 1.0×10^{12} cm^{-2} does not improve the transconductance significantly except for the PHEMT with a gate length of 70 nm. When contact resistances (which have been assumed to be the same as for the 120 nm single-doped PHEMT) are included into calculations, the magnitude of the transconductances reduce but the relative scale of improvement remains the same.

4. Impact ionization and gate tunnelling

The range of working voltages for sub-100 nm PHEMTs is likely to be restricted by impact ionization [13,15]. As the applied bias on the scaled device increases impact ionization may occur due to increasing number of highly energetic carriers. The turning of impact ionization into an avalanche triggers device breakdown. The breakdown is facilitated by the impact ionization created holes which lower the source-to-channel potential barrier introducing positive feedback for the drain current [38,39].

A second mechanism which introduces leakage and may trigger premature breakdown is the gate tunnelling since the gate-to-channel distance is reduced in the scaling process. It can initiate impact ionization at lower drain voltages since carriers which tunnel into the device will be highly energetic. The gate leakage may affect also the RF performance of the scaled PHEMTs.

Since hole dynamics [38,39] and the corresponding bipolar effects are not included in H2F/MC, the experimentally observed increase in the drain current at breakdown cannot be reproduced in our simulations. Instead, we calculate the impact ionization and gate tunnelling assisted increase in the electron current of the devices. This allows us to define the bias conditions corresponding to the onset of impact ionization which is determined only by the electron dynamics. The fact that the impact ionization threshold is not affected by hole dynamics has been verified by MC simulations in Ref. [39] (see Fig. 4 therein).

The additional drain current $I_{\mathrm{D}}^{\mathrm{assist}}$ corresponding to both impact ionization and thermionic tunnelling is calculated from the number, N, of impacted or tunnelled superparticles during the simulation time, t, as [40]

$$I_{\mathrm{D}}^{\mathrm{assist}} = N\frac{e_{\mathrm{S}}}{t}, \tag{4}$$

where e_{S} is the charge of a superparticle. To acquire statistically reliable impact ionization and tunnelling currents the MC device simulations have been run for 10 ps per bias point with a time step of 0.2 fs.

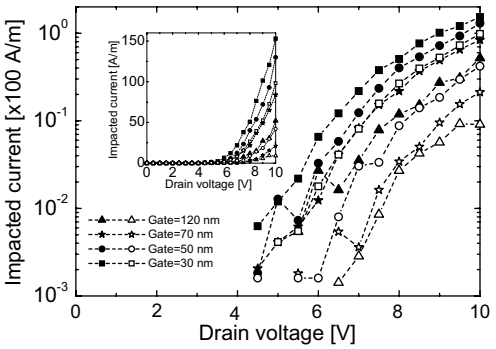

Fig. 11. Impact ionization assisted drain current versus the drain voltage at $V_G = -1.0$ V. The results obtained for the single-doped PHEMTs (open symbols) are compared to data for double-doped PHEMTs with the second DDL below the channel (full symbols). The optimal concentration of the additional DDL was found to be 2×10^{12} cm^{-2}.

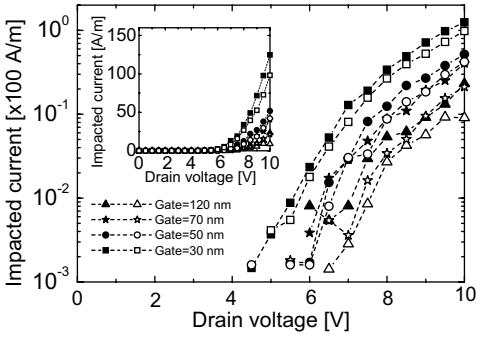

Fig. 12. Impact ionization current versus the drain voltage at the gate voltage of −1.0 V for the double doped scaled PHEMTs with the second DDL above the original doping. The concentration of this second DDL is again set to be 2×10^{12} cm^{-2}. The open symbols show results for the single-doped transistors.

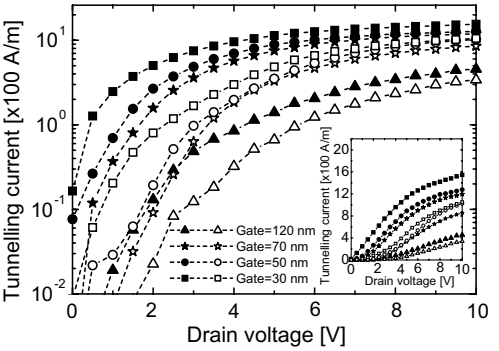

Fig. 13. Thermionic tunnelling assisted gate current versus the drain voltage again at $V_G = -1.0$ V. The tunnelling current in single delta doped structures (open symbols) is compared to the tunnelling current in the double-doped PHEMTs with the second DDL below the channel (full symbols).

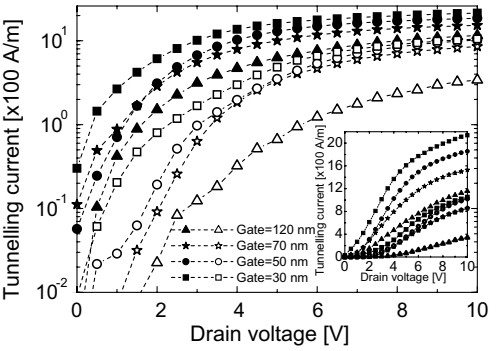

Fig. 14. Gate thermionic tunnelling versus the drain voltage at $V_G = -1.0$ V for the double doped scaled PHEMTs with the second DDL above the original doping layer, near to the gate. The distance of the second DDL from the original DDL is reduced from 8.5 nm to 4.5, 3.5, and 2.0 nm when a gate length is scaled down from 120 nm to 70, 50 and 30 nm, respectively. The data labelled with open symbols are for the single-doped PHEMTs.

The assisted drain current is examined in double doped scaled PHEMTs for both possible placements of the second DDL. The drain current purely due to impact ionization is plotted in Figs. 11 and 12 as a function of the applied drain voltage at a gate bias of −1.0 V for double-doped PHEMTs with the second DDL placed either below or above the original doping, respectively. The impact ionization drain current obtained from the single delta doped PHEMT are also shown in both Figs. 11 and 12 for comparison. As expected the simulated impact ionization current grows nearly exponentially with the applied drain bias [38]. Figs. 13 and 14 show the thermionic tunnelling gate current as a function of the drain voltage for the two DDL placements simulated also at −1.0 V gate bias. Open symbols in Figs. 13 and 14 refer to the thermionic tunnelling gate current obtained in the single delta doped structures. The gate current due to thermionic tunnelling has a different drain voltage dependence compared to the impact ionization current; it increases relatively sharply at lower drain voltages [15] but saturates rapidly at larger drain voltages.

The thresholds defined at a particular current level for both impact ionization and thermionic tunnelling decrease with device scaling. The threshold for the impact ionization drain current in those double-doped PHEMTs with the second delta doping below the channel is very similar to those obtained for single-doped PHEMTs [41]. However, the thresholds for the impact ionization assisted drain current for those

PHEMTs with the second DDL above the original doping are shifted towards lower drain voltages compared to the single-doped PHEMTs and those devices with the second DDL behind the channel. The placement of the second delta doping above the original DDL sharpens the fringing effects around the gate and the corresponding electric field at the drain end of the channel. This in turn increases the probability for an impact ionization event. Rather surprisingly for the two types of devices the ionization threshold at current level 1 A/m falls by less than 1.5 V when the devices are scaled from 120 to 30 nm channel length. It remains well above 4.0 V in the 30 nm transistor. A 'dead space effect' [39] with a width of nearly 10 nm is also observed on the drain side of the devices. The dead space effect occurs because electrons undergo impact ionization events not at the position of electric fringing fields but at much larger distances from the drain edge of the gate.

Figs. 13 and 14 show that although the thermionic tunnelling assisted gate current starts at a very low drain voltage, it rapidly saturates at large drain voltages [42] even for devices with very small gate-to-channel separation. Unfortunately, the level at which the tunnelling current saturates is comparable to the typical drain current at which the devices operate. When the second delta doping is placed below the channel it has no pronounced effect on the gate tunnelling current compared to the single-doped device [41]. Therefore, the gate tunnelling current in devices with this second DDL placement is no further cause for concern in the proportional scaling process. The placement of the second DDL near to the gate (Fig. 14) causes an increase in the thermionic tunnelling gate current compared to the design with a single DDL or a second DDL below the channel (Fig. 13). This is associated with the increase in the electrical fields due to the placement of an additional charge closer to the gate which reduces the width of the tunnelling barrier. Also the gate tunnelling current in those PHEMTs with the second DDL behind the channel is much lower at the 120 nm gate length. It then rapidly increases as the gate length is scaled to 70 nm and at the 50 and 30 nm gate lengths reaches the same level as in those PHEMTs with the second DDL above the original doping. The gate tunnelling current becomes a rather serious problem for the proportional scaling of PHEMTs to decananometre dimensions because it will trigger impact ionization and will initiate device breakdown at lower threshold voltages, as shown in Figs. 11 and 12 [41]. An alternative solution would be to use a high-κ dielectric layer above DDL to reduce the tunnelling [43].

The impact ionization and gate tunnelling currents depicted in Figs. 11–14 were simulated by the MC/H2F up to the drain voltage of 10 V. At the corresponding high electric fields the use of the nonparabolic analytical bandstructure model fails due to the high energies which carriers may reach. The introduction of the less-than-unity form factor [4] extends the validity of the analytical band model implemented in the H2F/MC up to an energy of 1.0 eV along the Γ–X valley direction in the E–$\mathbf{k}$ space and up to 2.0 eV along the Γ–L valley direction when compared to full bandstructure calculation based on the nonlocal pseudopotential method [44]. The nonparabolic analytical bandstructure model correctly describes the electron transport up to a particle energy of 2.0 eV and can be used to study the impact ionization even in materials with a narrow bandgap as $In_{0.53}Ga_{0.47}As$ [20]. Therefore, we have monitored the energies of all particles during the whole simulation at each time step to determine the number of particles which may violate the valid range for the nonparabolic analytical bandstructure model. We have found that only 8% of particles have reached an energy larger than 2.0 eV at a maximum considered drain bias of 10 V during the simulation of the impact ionization for the smallest, 30 nm gate length, PHEMT [41]. This is sufficient accuracy for our goal to find the drain threshold voltage for the start of impact ionization as well as to calculate the gate tunnelling current in order to determine the operating voltage of the scaled PHEMTs.

5. Conclusions

The effect of two possible placements of the second additional DDL into the PHEMT structure on the device performance has been studied using MC device simulations. The double-doped PHEMTs have been proportionally scaled from 120 to 70, 50 and 30 nm in order to improve their performance. In addition two mechanisms, impact ionization and gate thermionic tunnelling, which are likely to initiate breakdown in the scaled devices, have been investigated for the two double-doped designs.

The placement of the second DDL channels below the channel increases the drive current and improves the linearity while the transconductance remains practically the same. The placement of the second DDL above the channel, near to the gate, increases the drive current and also improves the transconductance. In this case the increase in the intrinsic transconductance is about 45% for the 120 nm gate length device (from 670 to 970 mS/mm), 32% for the 70 nm one (from 935 to 1235 mS/mm), 29% for the 50 nm one (from 1105 to 1427 mS/mm), and 34% for the smallest, 30 nm gate length device (from 1480 to 1998 mS/mm).

The threshold for impact ionization is practically the same for the double doped scaled PHEMTs with the second DDL below the channel as for the single doped scaled devices. This double-doped design is also less affected by gate tunnelling with gate tunnelling currents being very similar to those obtained for the single-doped

PHEMTs. The situation is a somewhat worse for the double-doped PHEMTs with the second delta doping above the original DDL. The impact ionization threshold in this case is lower compared to the other double-doped design and to single-doped devices. Also the gate tunnelling current increases due to higher electric fields close to the device gate caused by the vicinity of the second DDL.

Acknowledgement

This work has been supported by EPSRC under Grant No. GR/M93383.

References

[1] Yamashita Y, Endoh A, Shinohara K, Hikosaka K, Matsui T, Hiyamizu S, et al. Pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs with an ultrahigh f_T of 562 GHz. IEEE Electron Device Lett 2002;23:573–5.

[2] Suemitsu T, Yokoyama H, Ishii T, Enoki T, Meneghesso G, Zanoni E. 30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs. IEEE Trans Electron Devices 2002;49:1694–700.

[3] Shinohara K, Yamashita Y, Endo A, Hikosara K, Matsui T, Mimura T, et al. Extremely high-speed lattice-matched InGaAs/InAlAs high electron mobility transistors with 472 GHz cutoff frequency. Jpn J Appl Phys 2002;41:L437–9.

[4] Kalna K, Roy S, Asenov A, Elgaid K, Thayne I. Scaling of pseudomorphic high electron mobility transistors to decanano dimensions. Solid-State Electron 2002;46:631–8.

[5] Kalna K, Asenov A, Elgaid K, Thayne I. Scaling of pHEMTs to decanano dimensions. VLSI Design 2001; 13:435–9.

[6] Kizilyalli IC, Hess K, Larson JL, Widinger JD. Scaling properties of high electron mobility transistors. IEEE Trans Electron Devices 1986;33:1427–33.

[7] Dollfus P, Bru C, Hesto P. Monte Carlo simulation of pseudomorphic InGaAs/GaAs high electron mobility transistors: physical limitations at ultrashort gate length. J Appl Phys 1993;73:804–12.

[8] Hur KY, Hetzler KT, McTaggart RA, Vye DW, Lemonias PJ, Hoke WE. Ultralinear double pulse doped AlInAs/GaInAs/InP HEMTs. Electron Lett 1996;32:1516–8.

[9] Hur KY, Hetzler KT, McTaggart RA, Lemonias PJ, Hoke WE. Effect of channel thickness on linearity of double pulse doped AlInAs/GaInAs/InP HEMTs. Electron Lett 1997;33:331–2.

[10] Lin K-W, Yu K, Chang W, Cheng C, Lin K-P, Yen C, et al. Characteristics and comparison of $In_{0.49}Ga_{0.51}P/InGaAs$ single and double-doped pseudomorphic high electron mobility transistors. Solid-State Electron 2001;45:309–14.

[11] Sexl M, Böhm G, Xu D, Heiß H, Kraus S, Tränkle G, et al. MBE growth of double-sided doped InAlAs/InGaAs HEMTs with an InAs layer inserted in the channel. J Cryst Growth 1997;175/176:915–8.

[12] Sleinam A, Di Carlo A, Lugli P, Zandler G. Breakdown quenching in high electron mobility transistors by using body contact. IEEE Trans Electron Devices 2001;48:2188–91.

[13] Canali C, Paccagnella A, Pisoni P, Tedesco C, Relaroli P, Zanoni E. Impact ionization phenomena in AlGaAs/GaAs HEMTs. IEEE Trans Electron Devices 1991;38:2571–3.

[14] Li HP, Hartin OL, Ray M. An updated temperature-dependent breakdown coupling model including both impact ionization and tunneling mechanisms for AlGaAs/InGaAs HEMTs. IEEE Trans Electron Devices 2002; 49:1675–8.

[15] Somerville MH, Putnam CS, del Alamo JA. Determining dominant breakdown mechanisms in InP HEMTs. IEEE Electron Device Lett 2001;22:565–7.

[16] Babiker S, Asenov A, Roy S, Beaumont SP. Strain engineered pHEMTs on virtual substrates: a Monte Carlo simulation study. Solid-State Electron 1999;43:1281–8.

[17] Babiker S, Asenov A, Barker JR, Beaumont SP. Finite element Monte Carlo simulation of recess gate compound FETs. Solid-State Electron 1996;39:629–35.

[18] Stobbe M, Redmer R, Schattke W. Impact ionization rate in GaAs. Phys Rev B 1994;49:4494–500.

[19] Harrison D, Abram RA, Brand S. Characteristics of impact ionization rates in direct and indirect gap semiconductors. J Appl Phys 1999;85:8186–92.

[20] Isler M. Phonon-assisted impact ionization of electrons in $In_{0.57}Ga_{0.43}As$. Phys Rev B 2001;63:115209-1–8.

[21] Fischetti MV, Laux SE. Monte-Carlo electron transport in small semiconductor devices including band-structure and space-charge effects. Phys Rev B 1988;38:9721–45.

[22] Wordelman CJ. 3-D granular Monte Carlo simulations of semiconductor devices. PhD thesis. Urbana, IL; 2000. p. 13.

[23] Shabde SN, Yeh C. Ionization rates in $(Al_xGa_{1-x})As$. J Appl Phys 1970;41:4743–4.

[24] Law HD, Lee CA. Interband scattering effects on secondary ionization coefficients in GaAs. Solid-State Electron 1978;21:331–40.

[25] Pearsall TP, Capasso F, Nahory RE, Pollack MA, Chelikowsky JR. The band structure dependence of impact ionization by hot carriers in semiconductors: GaAs. Solid-State Electron 1978;21:297–302.

[26] Fischetti MV. Monte Carlo simulations in technologically significant semiconductors of the diamond and zinc-blende structures-part I: homogeneous transport. IEEE Trans Electron Devices 1991;38:634–48.

[27] Ritter D, Hamm RA, Feygenson A, Panish MB. Anomalous electric field and temperature dependence of collector multiplication in $InP/Ga_{0.47}In_{0.53}As$ heterojunction bipolar transistors. Appl Phys Lett 1992;60:3150–2.

[28] Pearsall TP. Impact ionization rates for electron and holes in $In_{0.53}Ga_{0.47}As$. Appl Phys Lett 1980;36:218–20.

[29] Kalna K, Asenov A, Elgaid K, Thayne I. Effect of impact ionization in scaled pHEMTs. In: Thayne I, editor. Proc. EDMO 2000. Glasgow; 2000. p. 236–41.

[30] Bude J, Hess K. Thresholds of impact ionization in semiconductors. J Appl Phys 1992;72:3554–61.

[31] Roy DK. Quantum mechanical tunnelling and its applications. New York: World Scientific; 1986. p. 17.

[32] Singh J. Semiconductor devices: basic principles. New York: John Wiley; 2001. p. 514.

[33] Winstead B, Ravaioli U. Simulation of Schottky barrier MOSFET's with a coupled quantum injection/Monte Carlo technique. IEEE Trans Electron Devices 2000;47:1241–6.

[34] Foisy MC, Tasker PJ, Hughes B, Eastman LF. The role of inefficient charge modulation in limiting the current-gain cutoff frequency of the MODFET. IEEE Trans Electron Devices 1988;35:871–8.

[35] Babiker S, Asenov A, Cameron N, Beaumont SP. A simple approach to include external resistances in the Monte Carlo simulation of MESFETs and HEMTs. IEEE Trans Electron Devices 1996;43:2032–4.

[36] Mateos J, Gonzáles T, Pardo D, Hoel V, Cappy A. Monte Carlo simulation of electronic characteristics in short channel δ-doped AlInAs/GaInAs HEMTs. Microelectron Reliab 2001;41:73–7.

[37] Moran DAJ, Kalna K, Boyd E, McEwan F, Mclelland H, Zhuang LL, et al. Self-aligned 0.12 μm T-gate $In_{.53}Ga_{.47}As$/$In_{.52}Ga_{.48}As$ technology using a non-annealed ohmic contact strategy. In: Franca J, Freitas P, editors. Proc. 33rd European Solid-State Device Research Conference (ESSDERC). Estoril; 2003. p. 315–8.

[38] Canali C, Pavan P, Di Carlo A, Lugli P, Malik R, Manfredi M, et al. Experimental and Monte Carlo analysis of impact-ionization in AlGaAs/GaAs HBT's. IEEE Trans Electron Devices 1996;43:1769–77.

[39] Di Carlo A, Rossi L, Lugli P, Zandler G, Meneghesso G, Jackson M, et al. Monte Carlo study of the dynamic breakdown effects in HEMT's. IEEE Electron Device Lett 2000;21:149–51.

[40] Moglestue C. Monte Carlo simulation of semiconductor devices. London: Chapman & Hall; 1993. p. 188.

[41] Kalna K, Asenov A. Gate tunnelling and impact ionisation in sub-100 nm PHEMTs. IEICE Trans Electron 2003;E86-C:330–5.

[42] Li HP, Hartin OL, Ray M. An updated temperature-dependent coupling model including both impact ionization and tunnelling mechanisms for AlGaAs/InGaAs HEMTs. IEEE Trans Electron Devices 2002;49:1675–8.

[43] Rotondaro ALP, Visokay MR, Shanware VA, Chambers JJ, Colombo L. Carrier mobility in MOSFETs fabricated with Hf–Si–O–N gate dielectric, polysilicon gate electrode, and self-aligned source and drain. IEEE Electron Device Lett 2002;10:603–5.

[44] Chelikowsky JR, Cohen ML. Nonlocal pseudopotential calculations for the electronic structure of eleven diamond and zinc-blende semiconductors. Phys Rev B 1976;14:556–82.