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Monte Carlo Simulation of Implant Free InGaAs MOSFET

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Abstract. The performance potential of *n*-type implant free $In_{0.25}Ga_{0.75}As$ MOSFETs with high-κ dielectric is investigated using ensemble Monte Carlo device simulations. The implant free MOSFET concept takes advantage of the high mobility in III-V materials to allow operation at very high speed and low power. A 100 nm gate length implant free $In_{0.25}Ga_{0.75}As$ MOSFET with a layer structure derived from heterojunction transistors may deliver a drive current of 1800 A/m and transconductance up to 1342 mS/mm. This implant free transistor is then scaled in the both lateral and vertical dimensions to gate lengths of 70 and 50 nm. The scaled devices exhibit continuous improvement in the drive current up to 2600 A/m and 3259 A/m and transconductance of 2076 mS/mm and 3192 mS/mm, respectively. This demonstrates the excellent scaling potential of the implant free MOSFET concept.

1. Introduction

Recent research into new device architectures and materials [1] has revived the idea to employ high electron mobility III-V semiconductors in MOS devices [2]. The development of a suitable high-κ gate dielectric for GaAs with an 'unpinned' oxide/semiconductor interface [3] has given this notion a further momentum. Monte Carlo (MC) device simulations of ion-implanted III-V MOSFETs have predicted that $In_{0.2}Ga_{0.8}As$ MOSFETs with 80 nm metallurgical gate length would outperform the equivalent Si and strained Si devices [4, 5]. However, when the ion-implanted transistor based on the $In_{0.2}Ga_{0.8}As$ channel is scaled down to a metallurgical gate length of 35 nm the performance margin to the equivalent Si based MOSFETs shrinks [4, 5]. Therefore, the introduction of III-V materials in MOSFETs requires new device concepts which enjoy the benefit of scaling while maintaining a high electron mobility. One of these recently proposed new concepts [6] is an enhancement mode MOSFET which does not require implanted source/drain regions and extensions.

2. Implant free MOSFETs

Fig. 1 illustrates an implant free MOSFET based on an epitaxial layer structure derived from high electron mobility transistors. The structure comprises a gate oxide, source and drain Ohmic contacts, and a metal gate electrode with a high workfunction. The source-gate and gate-drain regions are normally "on" and conducting under flatband conditions. The gate region is designed to be non-conducting at zero gate voltage for normally "off" operation.

In this work, we have studied the potential performance of an *n*-type implant free MOSFET with an $In_{0.25}Ga_{0.75}As$ channel, a 100 nm gate length and a high-κ gate dielectric, shown in Fig. 1, using

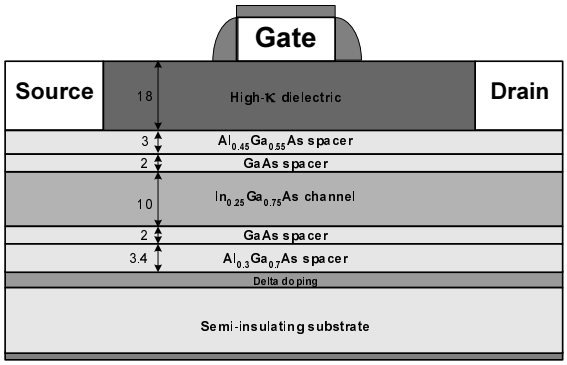

Fig. 1: Cross-section scheme illustrating an implant-free enhancement mode MOSFET.

Thickness of	Gate length [nm] 100	70	50
High-κ dielectric [nm]	18	13	9
GaAs [nm]	1	0.5	0.5
AlGaAs spacer [nm]	3	1.5	1
GaAs embed [nm]	2	1.5	1
InGaAs spacer [nm]	10	7	5
GaAs embed [nm]	2	1.5	1
AlGaAs doping spacer [nm]	3.4	2.4	1.7
δ-doping concentration [$\times 10^{12}$ cm^{-2}]	2.65	3.5	4.25

Table I: Layer dimensions and δ-doping concentrations for the implant free MOSFETs scaled with respect of given gate lengths.

our ensemble Monte Carlo (MC) device simulator [7]. The MC simulator has an extended transport model which features Fermi-Dirac (F-D) statistics. The F-D statistics are implemented by calculating self-consistently the Fermi energy and the electron temperature [8] from the known electron density and the average electron energy at each mesh point during every MC time step. The obtained Fermi energy and electron temperature are subsequently used in each scattering process to evaluate the occupation of a final state and to calculate the static screening length in ionized impurity scattering. For comparison, simulations of the intrinsic performance of the implant free transistors have been also carried out assuming that the final state is always empty. These This results are referred to as Boltzmann statistics.

The 100 nm gate length implant free MOSFET is then scaled in both vertical and horizontal directions with respect to gate lengths of 70 and 50 nm, as depicted in Table I, to evaluate the scaling potential of the enhancement mode implant free concept. In addition, we have also increased the δ-doping concentration in the scaled devices as given in Table I in order to keep the threshold voltage V_{th} close to that of the 100 nm gate length variant.

Fig. 2 shows I_D-V_G characteristics for a 100 nm implant free $In_{0.25}Ga_{0.75}As$ MOSFET with 100 nm

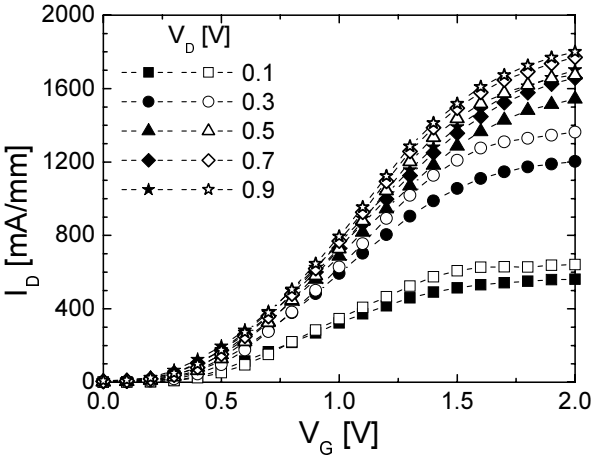

Fig. 2: I_D-V_G characteristics at indicated drain voltages for the 100 nm implant free $In_{0.25}Ga_{0.75}As$ MOSFET. The source-to-gate and the gate-to-drain distances are assumed to be 100 nm.

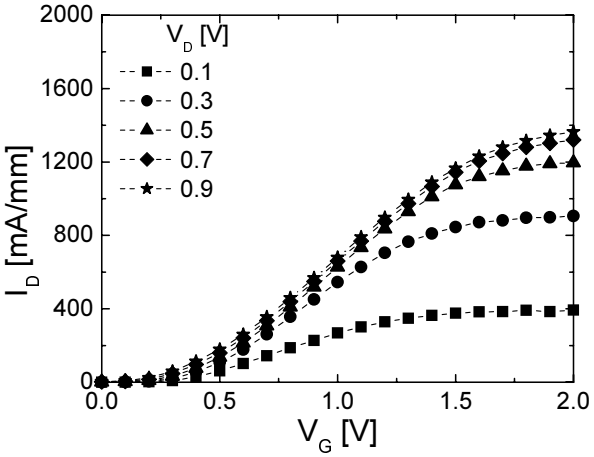

Fig. 3: I_D-V_G characteristics of the same, 100 nm implant free InGaAs MOSFET, as in Fig. 2, when the source-to-gate and the gate-to-drain distances increase to 200 nm.

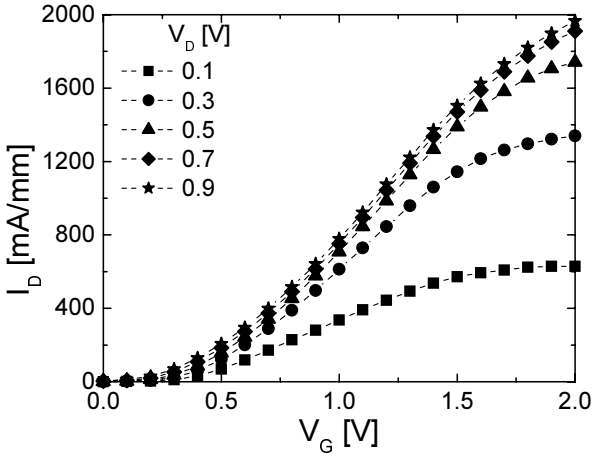

Fig. 4: I_D-V_G characteristics of the same, 100 nm implant free InGaAs MOSFET, as in Fig. 2, when the source-to-gate and the gate-to-drain distances decrease to 50 nm.

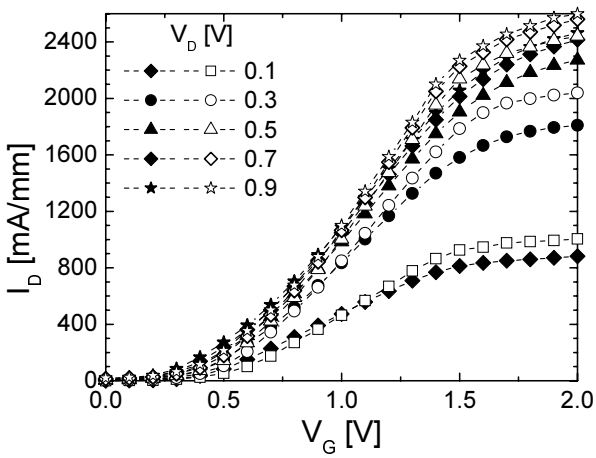

Fig. 5: I_D-V_G characteristics at indicated V_D of the 70 nm gate length implant free $In_{0.25}Ga_{0.75}As$ MOSFET. The source-to-gate and gate-to-drain distances are also scaled to 70 nm.

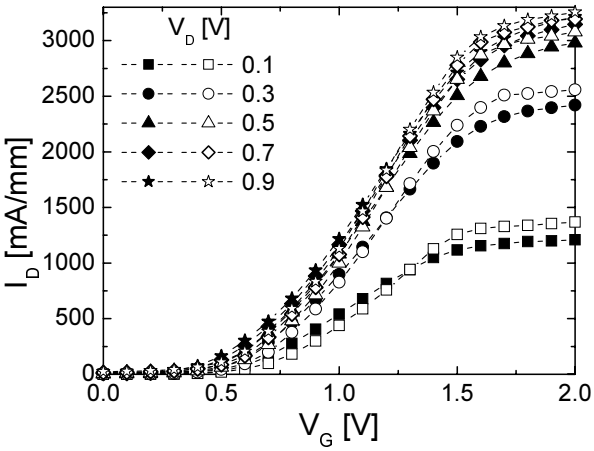

Fig. 6: I_D-V_G characteristics at various V_D of the 50 nm gate length implant free $In_{0.25}Ga_{0.75}As$ MOSFET. The source-to-gate and the gate-to-drain distances are 50 nm.

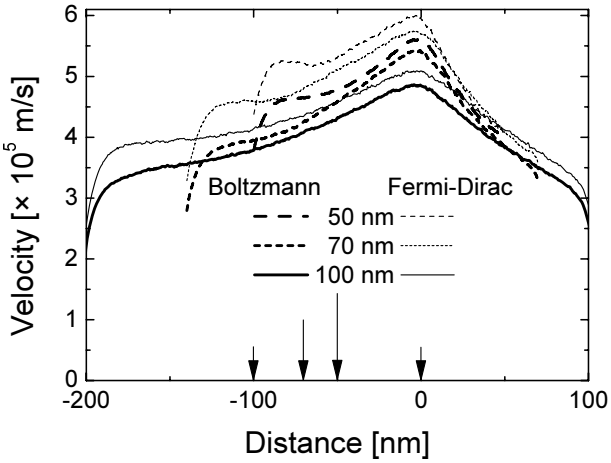

Fig. 7: Average electron velocity along the channel of scaled implant free MOSFETs at V_G-V_{th}=1.3 V and V_D=0.7 V. The beginning of the gate is depicted by arrows while the end of the gate is always set at zero.

source-to-gate (L_{GS}) and gate-to-drain (L_{GD}) separations. The full symbols represent the intrinsic drain current obtained using Boltzmann statistics while the open symbols show results obtained using self-consistent F-D statistics. The drain current rapidly increases when the drain voltage changes from 0.1 V to 0.3 V. This increase is reduced at a drain voltage of 0.5 V and eventually, I_D saturates at V_D=0.7 V.

The L_{GS} and L_{GD} separations which determine the parasitics access resistances in the device are a crucial factor limiting the drive current in small devices. Therefore, we have carefully examined their effect on drive current. When L_{GS} and L_{GD} are increased from 100 nm to 200 nm, the drain current is reduced by approximately 15 % as illustrated in Fig. 3. However, Fig. 4 shows that when these separations are reduced to 50 nm the drain current increases by approximately 10 %.

The scaling of the implant free MOSFETs to 70 nm and 50 nm can deliver a large improvement of 50 % and 90 % in the device performance, respectively, as shown in Figs. 5 and 6. Again, the results obtained using Boltzmann statistics (full symbols) and using F-D statistics (open symbols) are compared. Figs. 5

and 6 show that the implant free $In_{0.25}Ga_{0.75}As$ MOSFET can be effectively scaled down to achieve a large performance improvement. It also becomes apparent from Figs. 5 and 6 that the difference between

Boltzmann and F-D statistics increases with increasing drain voltage and that F-D statistics give a slightly larger drain current by approximately 12% (at $V_D = 0.3$ V) for the 100 nm and 70 nm gate lengths MOSFETs. In the case of the 50 nm gate length $In_{0.25}Ga_{0.75}As$ MOSFET, the effect of F-D statistics becomes negligible with only 5% difference between the drain current obtained using Boltzmann statistics and F-D statistics.

The relatively smooth I_D-V_G characteristics allow the calculation of the intrinsic transconductance at various applied drain voltages. The 100 nm implant free MOSFET exhibits a maximum intrinsic transconductance of 1340 mS/mm. When the device is scaled to gate length of 70 nm and 50 nm, the maximum intrinsic transconductance increases to 2080 mS/mm and 3190 mS/mm, respectively. The continuous increase in the transconductance is another indicator that the implant free concepts is suitable for further scaling into deep sub-100 nm dimensions.

Finally, Fig. 7 shows the average electron velocity along the $In_{0.25}Ga_{0.75}As$ channel in scaled implant free MOSFETs. This figure illustrates that electrons quickly gain a high velocity which peaks at $4.8 \times 10^5 m/s$ ($5.1 \times 10^5 m/s$) in the 100 nm device when using Boltzmann statistics (using self-consistent F-D statistics) and can further increase up to $5.4 \times 10^5 m/s$ ($5.7 \times 10^5 m/s$) and to $5.6 \times 10^5 m/s$ ($6.0 \times 10^5 m/s$) with scaling of the gate length to 70 nm and 50 nm, respectively. However, the velocity increase is slightly suppressed in the scaled devices because the improved non-equilibrium electron transport is affected by enhanced scattering due to higher δ-doping concentrations.

3. Conclusions

A finite element heterostructure MC device simulator has been used to study the performance of implant free InGaAs MOSFETs. We have demonstrated that a 100 nm gate length implant free MOSFET with an $In_{0.25}Ga_{0.75}As$ channel and a high-κ gate oxide exhibits a drive current of 1650 mA/mm and a maximum transconductance of 1340 mS/mm. The MC device simulations employ a bulk MC transport model verified against experimental data obtained for GaAs, AlGaAs and InGaAs [7] and were calibrated against experimentally obtained I_D-V_D and I_D-V_G characteristics of various HEMTs [7]. The simulated electron mobility and sheet density in the implant free $In_{0.25}Ga_{0.75}As$ MOSFET were also verified against measurements on relevant epitaxial layers [9].

The implant free MOSFET has a significant scaling potential. When properly scaled in both vertical and lateral directions [7], the 70 nm gate length implant free $In_{0.25}Ga_{0.75}As$ MOSFET can deliver approximately 60% drain current increase and a maximum transconductance of 2080 mS/mm. When the device is further scaled down to the 50 nm gate length, the drain current increases by approximately $90 - 100\%$ compared to the drain current observed in the 100 nm implant free MOSFET while the maximum transconductance reaches 3190 mS/mm.

Acknowledgments

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References

[1] Wong H-S P 2002 *IBM J. Res. Dev.* **46** 133
[2] Kalna K, Yang L, and Asenov A 2005 Proc. Electronic Solid State and Device European Research Conf. ed S Cristoloveanu, M Brillouët and T Skotnicki (Grenoble) p 169
[3] Passlack M, 2005 *J. Vacuum Sci. Technol.* B**23** 1773
[4] Kalna K, Boriçi M, Yang L and Asenov A 2004 *Semicond. Sci. Technol.* **19** S202
[5] Fischetti M V, Laux S E, Solomon P M and Kumar A 2005 *J. Comput. Electron.* **3** 287
[6] Passlack M, Hartin O, Ray M and Medendorp N 2004 *US Patent 6,963,090 2005*
[7] Kalna K, Roy S, Asenov A, Elgaid K and Thayne I 2002 *Solid-State Electron.* **46** 631
[8] Kalna K, Passlack M and Asenov A 2005 submitted to *IEEE Trans. Electron Devices*
[9] Passlack M, Droopad R, Rajagopalan K, Abrokwah J, Gregory R, and Nguyen D, *IEEE Electron Device Letters* **26** 713