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Semicond. Sci. Technol. **19** (2004) S202–S205 PII: S0268-1242(04)72227-0

Monte Carlo simulations of III–V MOSFETs

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Received 28 July 2003
Published 5 March 2004
Online at stacks.iop.org/SST/19/S202 (DOI: 10.1088/0268-1242/19/4/069)

Abstract

The performance potential of an 80 nm physical gate length MOSFET with GaAs channel and high-k gate insulator is investigated using Monte Carlo simulations. The results show that such a device could deliver a 100–125% increase in the drive current at both low and high drain biases compared to equivalent Si based MOSFETs. Various transport model enhancements including the Fermi–Dirac statistics and the interface roughness scattering have been systematically studied in order to attain a more realistic prediction of the device performance.

1. Introduction

The semiconductor industry faces new challenges while foreseeing the end of scaling for a standard Si MOSFET. Possible solutions include the introduction of high-k dielectrics in the gate stack of Si MOSFETs [1]; the intention of companies such as IBM [2] and Intel to integrate the epitaxial SiGe in conventional CMOS; and the extensive research into alternative device architectures such as thin SOI [3], double [4] and FIN gate [5] MOSFETs. Si wafers with GaAs on top of $SrTiO_3$ [6] or Ge buffers offer further scenarios for integrating very fast digital compound MOSFETs with optical components and less demanding Si blocks on a single chip. Both MESFETs [6] and HEMTs [7] have been demonstrated using this technology. Good properties of the interface between dielectric and III–V semiconductor (Ga_2O_3/AlGaAs) have also been reported in a GaAs p-channel MOSFET [8].

We extensively study the potential performance of an n-type GaAs channel MOSFET using ensemble Monte Carlo (MC) simulations [9]. The investigated GaAs MOSFET is assumed to have a physical gate length of 80 nm and a high-k gate dielectric which may be achieved within emerging technologies as illustrated in figure 1. The transport model used in MC device simulations has been extended with Fermi–Dirac (FD) statistics for the screening in ionized impurity scattering and the Fermi exclusion principle (degeneracy) in every scattering process. Further, we have adopted the interface roughness scattering [10] and the effective potential (EP) [11] to incorporate the effect of mobility degradation and the quantum confinement at the dielectric/semiconductor interface. The simulated device performance has been compared with the performances of n-type 67 nm conventional and strained Si channel MOSFETs reported by IBM [2].

2. Device simulation approach

The simulations of the III–V MOSFETs have been carried out using the MC compound semiconductor simulator H2F/MC described in detail elsewhere [13, 14]. The MC module includes electron scattering with polar optical phonons, inter- and intra-valley optical phonons, non-polar optical phonons, acoustic phonons and ionized impurity scattering. All scattering rates and the generation of final states are modified with the nonunity form factor [15] within a non-parabolic band approximation. The MC device simulator was calibrated against both I_D–V_G and I_D–V_D characteristics of a 120 nm pseudomorphic HEMT fabricated and measured at the University of Glasgow [13]. Further, the MC simulator has been recently employed in the investigation of electron transport in a 120 nm double doped InGaAs/InAlAs lattice matched HEMT providing excellent agreement with measured I_D–V_D characteristics [16].

The GaAs MOSFETs replicate the structure, equivalent oxide thickness and doping profiles in the channel of the controlled IBM device which have been deduced from comprehensive Medici calibrations [17]. The peak n-type doping in the source/drain has been reduced to 5×10^{19} cm^{-3} to reflect the lower doping activation in GaAs. A time step of 0.1 fs has been used throughout the MC simulations (total time is 10 ps) in order to suppress noise coming from the highly doped source/drain. The mesh spacing along the GaAs channel is 1 nm in order to resolve the electron–electron interactions [18]. Figure 2 compares the intrinsic performance

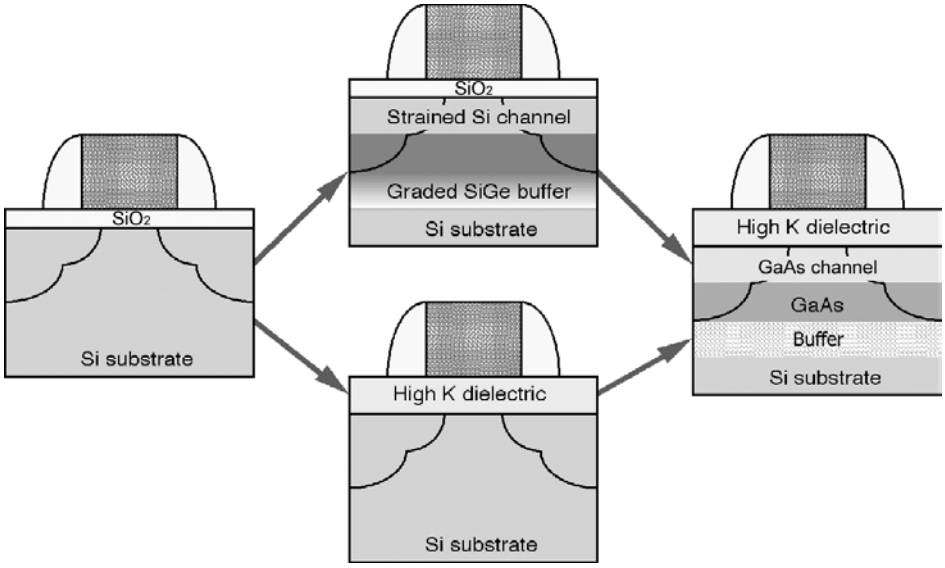

Figure 1. Concept of III–V channel MOSFETs with high-k gate dielectric utilizing GaAs on Si wafer technology.

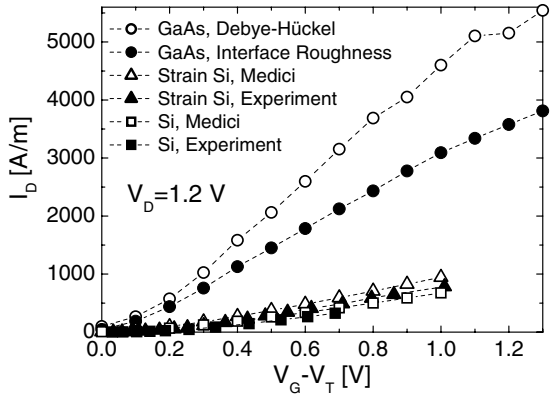

Figure 2. I_D–V_G characteristic of 80 nm GaAs MOSFETs compared to the strained Si and conventional Si MOSFETs, both with a 67 nm effective channel length. The MC simulations of the GaAs MOSFET are shown by circles. Medici simulations of the strained Si and Si MOSFETs are shown by open triangles and open squares, respectively, and represent an intrinsic device (source/drain contact resistances deembedded).

of the GaAs MOSFET obtained directly from MC simulations with 67 nm effective channel length conventional and strained Si MOSFETs [2] obtained from Medici simulations. The experimental I_D–V_G characteristics of Si based MOSFETs are also shown.

MOSFET devices based on III–V material may suffer from a lower DOS compared to those of Si [4]. Therefore, FD statistics have been included to obtain a more realistic estimate for the device performance even though the source/drain doping in the 80 nm GaAs MOSFET is lower than those in Si devices. The FD statistics are implemented via the static screening model used only in ionized impurity scattering and via the Fermi exclusion principle used after every scattering event. The inverse screening length, β, in the static screening model is defined by [19]

$$\beta^2 = \frac{n(\mathbf{r},t)\,e^2}{\varepsilon\,k_B T}\frac{\mathrm{F}_{-1/2}(\eta)}{\mathrm{F}_{1/2}(\eta)}, \tag{1}$$

where $\eta = [E_f(\mathbf{r},t) - E_c]/k_B T$ with E_f and E_c the Fermi energy and conduction band energy respectively, and ε the dielectric constant. F_α is the Fermi integral of order α. The MC simulations of bulk mobility in GaAs [20] have verified the screening model (1), especially when used with degeneracy, giving very good agreement with experimental data at very high ionized impurity concentrations.

Quantum confinement which occurs at the interface of the GaAs MOSFET should play a more important role than that in Si MOSFETs. The EP approach is therefore adopted since it can be rather easily applied to MC simulations. A classical potential P is convolved with a Gaussian distribution, G, to get an EP, P_{eff}, using the relation [11]

$$\begin{aligned} P_{\mathrm{eff}}(\mathbf{r}) &= \int \mathrm{d}\mathbf{r}'\,P(\mathbf{r}+\mathbf{r}')G(\mathbf{r}'), \\ G(\mathbf{x}) &= \frac{1}{a\sqrt{2\pi}}\exp\left(-\frac{x^2}{2a^2}\right), \end{aligned} \tag{2}$$

where a is a smoothing parameter. The parameter a, which was approximated by $\hbar/\sqrt{12mk_BT}$ [11], has been calibrated against a self-consistent Poisson–Schrödinger solution in the subthreshold region leading to $a = 1.6$ nm.

The interface roughness scattering model included in the MC device simulator is based on Ando's model with an exponential auto-correlation function (ACF) to define the properties of the dielectric/semiconductor interface [10]. Since the RMS height and the correlation length of the interface in the GaAs MOSFET are not known at the moment we have considered the worst possible case with an RMS height of 0.24 nm [8] and a correlation length of 1.7 nm typical for the SiO_2/Si interface.

The average velocity along the GaAs channel shown in figure 3 is several times higher than that in the Si device thanks to a lower effective mass and reduced scattering. When the EP (2) is employed together with degeneracy the peak of the average velocity will increase by further 20%. But when the interface roughness scattering is included into simulation the peak velocity is reduced by 30%. However, this

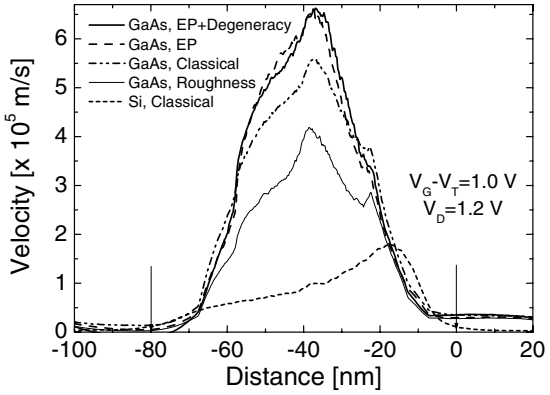

Figure 3. Average velocity along the 80 nm gate length GaAs channel MOSFETs compared to the velocity in the standard 67 nm effective channel length Si MOSFET shown by the short dash line. The static screening model has been employed in each simulation adding various model enhancements. The full line is a simulation with the effective potential and degeneracy, the dash line is with the effective potential only and the dash double dot line is a simulation with static screening model only. The thin line is with the Debye–Hückel screening and interface roughness. The beginning and end of the physical gate are depicted by arrows.

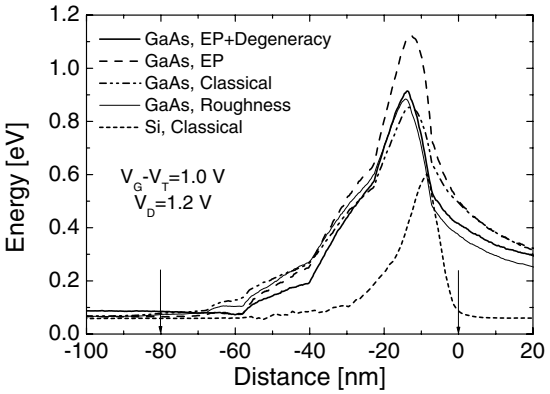

Figure 4. Average carrier energy along the channel of the 80 nm GaAs MOSFETs compared to an average energy in the equivalent Si MOSFET. The same model enhancements as in figure 3 are presented.

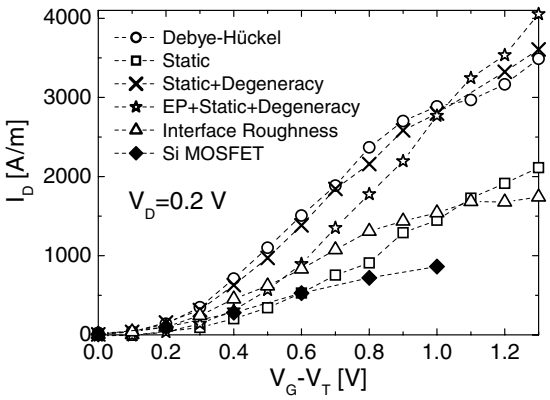

Figure 5. I_D–V_G characteristics of GaAs MOSFETs with a 80 nm physical gate length at a drain bias of 0.2 V for various transport model enhancements. Open circles are for the Debye–Hückel screening, open squares for the static screening model, crosses for both the static screening and degeneracy, open stars for the static screening, degeneracy and EP together and, finally, open triangles are for the interface roughness model and Debye–Hückel screening. The results obtained for the equivalent Si MOSFET with the interface roughness scattering excluded are also shown.

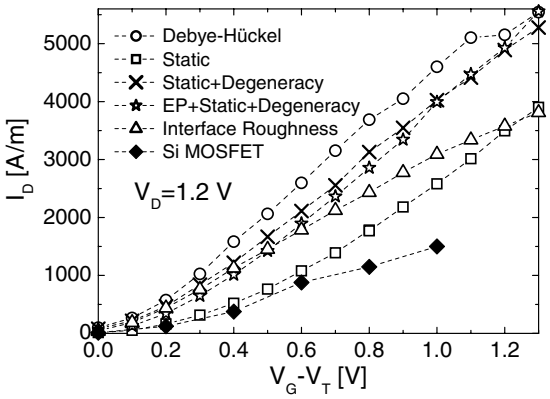

Figure 6. I_D–V_G characteristics of GaAs MOSFETs with a 80 nm physical gate length at a drain bias of 1.2 V for the same transport model enhancements as in figure 5. The MC simulations of the equivalent Si MOSFET in which the interface roughness scattering was omitted are again given for a comparison.

velocity is still significantly larger than that in the equivalent Si MOSFET which has also been simulated including the interface roughness scattering. The difference is particularly large at the source end of the channel which controls the drain current. The average energy along the channel shown in figure 4 behaves quite differently. When only the EP alone is employed in a MC simulation the energy of carriers will increase at the drain side of the gate by about 25% because a smoothing procedure of the EP pushes the conduction band to higher energies. The effect of all other enhancements on the carrier energy is rather small and the energy remains relatively close to the classical result when only the static screening model is employed.

Figures 5 and 6 show I_D–V_G characteristics at $V_D = 0.2$ V and 1.2 V, respectively, when various improvements to the transport model are included in MC simulations of the GaAs MOSFET. The static screening model (1) lowers the drain current compared to the Debye–Hückel screening by nearly 50%. However, if degeneracy is taken into account in the selection of the final state, together with screening (1), then the drain current increases due to the reduced scattering rate associated with a smaller number of final states. The introduction of EP (2) also reduces the drain current. When the EP is employed in the simulations in combination with screening (1) and degeneracy, the current is reduced by more than 20% to 30%. When the interface scattering model [10] is included in the simulations, the current decreases by approximately 50% at low drain voltage and approximately 30% at high drain voltage. Finally, the I_D–V_G characteristics of the equivalent Si MOSFET obtained when the interface roughness scattering is excluded in MC simulations [21] are given for a comparison. Nevertheless, even in this case, the GaAs MOSFET still gives more than a 100% improvement in the drive current at high drain voltage which is much greater than the 30% improvement observed in strained Si channel MOSFETs.

The higher mobility and reduced phonon scattering are responsible for a better performance of the GaAs MOSFET over the Si device at a low drain voltage of 0.2 V seen in figure 5, as has already been pointed out by Fischetti and Laux [12]. However, figure 6 shows that the 80 nm GaAs MOSFET should outperform the equivalent Si MOSFET also at $V_D = 1.2$ V. A better performance of the GaAs device at high drain voltages can no longer be attributed just to the higher mobility and reduced phonon scattering in GaAs [12]. The explanation may lay in the fact that the GaAs MOSFET in this work has one order of magnitude higher source/drain doping than those considered in [12] resulting in a lower access resistance. This is combined with higher injection velocity in the source end of the channel because the higher doping enhances the ionized impurity scattering which decreases the momentum relaxation time. Carriers then spend a longer time at the source/drain allowing them to relax to lower kinetic energies. It means that more carriers will be in the Gamma valley (with a lower effective mass) before entering the active region than those in the MOSFET with a source/drain doping of 10^{18} cm^{-3}.

3. Conclusions

Using ensemble MC device simulations we have demonstrated that compound sub-100 nm MOSFETs with a GaAs channel may deliver more than 100% improvement in the drive current compared to the present state of the art Si MOSFETs. We have found that the 80 nm GaAs MOSFET would outperform the equivalent Si MOSFET by more than 100% at high drain voltages (1.2 V).

The static screening model (1) used in the ionized impurity scattering process reduces the drive current by about 50% compared to the Debye–Hückel screening. However, when degeneracy is taken into account in every scattering event the drive current returns back to its original value. The EP (2) results in the drive current reduction by another 20–30%. Finally, the interface roughness scattering will further decrease the drive current by approximately 40% at high drain voltage. This still leaves the 80 nm GaAs MOSFET with a performance superiority over both equivalent strained and conventional Si MOSFETs. We would like to point out that while the better performance of the GaAs based MOSFETs has already been predicted at low drain voltages, previously published simulations show no significant benefits at high drain voltages compared to equivalent Si MOSFETs. We have attributed the improvement reported in this work to improved device design and particularly the use of higher *n*-type doping in the source/drain of our GaAs MOSFET.

Acknowledgment

This work has been supported by EPSRC under grant no GR/M93383.

References

[1] Akbar M S *et al* 2003 *Appl. Phys. Lett.* **37** 1757
[2] Rim K *et al* 2001 *Symp. on VLSI Technol., Dig. of Tech. Papers* **2001** 59
[3] Chau R, Kavalieros J, Doyle B, Murthy A, Paulsen N, Lionberger D, Barlage D, Arghavani R, Roberds B and Doczy M 2001 *Tech. Dig. Int. Electron Devices Meet.* **2001** 621
[4] Solomon P M and Laux S E 2001 *Tech. Dig. Int. Electron Devices Meet.* **2001** 95
[5] Kedzierski J *et al* 2001 *Tech. Dig. Int. Electron Devices Meet.* **2001** 437
[6] Eisenbeiser K, Emrick R, Droopad R, Yu Z, Finder J, Rockwell S, Holmes J, Overgaard C and Ooms W 2002 *IEEE Electron Device Lett.* **23** 300
[7] Hierl T, O'Steen M, Droopad R and Baklenov O 2002 *Proc. Int. Conf. on Solid State Devices and Materials (Nagoya, Japan)* p 280
[8] Passlack M, Abrokwah J K, Droopad R, Zhiyi Y, Overgaard C, Sang I Y, Hale M, Sexton J and Kummel A C 2002 *IEEE Electron Device Lett.* **23** 508
[9] Lebwohl P A and Price P J 1971 *Solid State Commun.* **9** 1221
[10] Ferry D K 2000 *Semiconductor Transport* (New York: Taylor and Francis) p 135
[11] Ferry D K 2000 *Superlatt. Microstruct.* **27** 61
[12] Fischetti M V and Laux S E 1991 *IEEE Trans. Electron Devices* **38** 650
[13] Kalna K, Roy S, Asenov A, Elgaid K and Thayne I 2002 *Solid-State Electron.* **46** 631
[14] Babiker S, Asenov A, Cameron N, Beaumont S P and Barker J R 1996 *IEEE Trans. Electron Devices* **43** 2032
[15] Matz D 1968 *Phys. Rev.* **168** 843
[16] Moran D A J, Kalna K, Boyd E, McEwan F, McLelland H, Zhuang L L, Stanley C R, Asenov A and Thayne I 2003 *Proc. 33rd Eur. Solid-State Device Research Conf. (ESSDERC) (Estoril, Portugal)* ed J Franca and P Freitas p 315
[17] Medici 1999 Manual 1999.2 Avanti Corporation
[18] Wordelman C J and Ravaioli U 2000 *IEEE Trans. Electron Devices* **47** 410
[19] Chattopadhyay D and Queisser H J 1981 *Rev. Mod. Phys.* **53** 745
[20] Kalna K, Yang L and Asenov A 2003 *J. Comput. Electron.* **2** 347
[21] Boriçi M, Watling J R, Wilkins R C W, Yang L, Barker J R and Asenov A 2003 *Semicond. Sci. Technol.* **19** S155