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Scaling of pseudomorphic high electron mobility transistors to decanano dimensions

K. Kalna *, S. Roy, A. Asenov, K. Elgaid, I. Thayne

Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK

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Abstract

The performance enhancement associated with the scaling of pseudomorphic high electron mobility transistors (PHEMTs) to deep decanano dimensions is studied using Monte Carlo (MC) simulations. The full scaling of a standard 120 nm PHEMT to gate lengths of 90, 70, 50 and 30 nm in both lateral and vertical dimensions is compared with an approach where only the lateral dimensions are scaled. The study is based on an extended transport module integrated in the finite element MC simulator H2F and accurate up to an electric field of 200 kV/cm, and on the careful calibration of MC device simulations against *I–V* characteristics from the real 120-nm gate length PHEMT. The fully scaled devices exhibit a continuous improvement in transconductance as channel lengths reduce while performance deteriorates in devices scaled only laterally. The contact resistances become a limiting factor to the performance of the fully scaled devices at shorter channel lengths. The microwave performance of the scaled devices is studied using the transient MC analysis.

Keywords: Pseudomorphic high electron mobility transistors; Scaling; Monte Carlo simulation; Transconductance; RF analysis

1. Introduction

Pseudomorphic high electron mobility transistors (PHEMTs) with low indium content channels and channel lengths of 0.25–0.15 μm are the workhorse of the MMIC industry [1]. Whilst today research into ultrafast compound FETs is mainly focused on high In content channel devices on InP or 'virtual' substrates with strain relief buffers [2], the more mature and cost-effective PHEMT technology based on low defect density and manufacturable GaAs substrates remains the preferred choice for mass market production. Although PHEMT technologies have historically led in channel length reduction and engineering of active layers, with Si MOSFETs approaching sub-0.1-μm gate lengths [3], there are new incentives for exploring the further potential and limitations of PHEMT scaling.

HEMT scaling has been the focus of several past simulation studies [4–6] encouraged by an expectation of improved transconductance and cut-off frequency. However, most of these only consider scaling in lateral dimensions [4,7], keeping the gate to channel separation constant, which inevitably results in erosion of the gain associated with scaling due to a loss of charge control from the gate [4]. Most of the simulations have also been constrained to devices with oversimplified geometries and do not take account of the impact of the gate recess, gate shape, and contact and access resistances on device parasitics and RF performance.

We present a detailed simulation study of the expected improvements in the performance of conventional PHEMT devices scaled to decanano dimensions. Starting with a conventionally fabricated and characterized 120 nm PHEMT, the simulated PHEMTs are scaled down in proportion to gate lengths of 90, 70, 50 and 30 nm. Important to this work is that the devices are shrunk not only in the lateral but also in the vertical dimensions. The real device geometry and the corresponding parasitics are also properly included in the

* Corresponding author.
E-mail address: kalna@elec.gla.ac.uk (K. Kalna).

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simulations. We demonstrate that when scaling is performed in the lateral dimensions only there is no improvement in the performance of PHEMTs with gate lengths less than 100 nm as already shown in Refs. [4,7].

The scaling study is based on a thorough calibration of our Monte Carlo (MC) device simulator against experimental data for a 120-nm gate length PHEMT fabricated at the University of Glasgow. The validity of the analytical MC simulator is extended to cover the high electric fields expected in aggressively scaled devices. We study DC and RF performance of the scaled devices in detail focusing on the detrimental effects of device parasitics.

The essential features of the MC module included in our device simulator are described in Section 2, in which we also present the calibration of the transport models against velocity field characteristics of the relevant composite materials. Section 3 describes the calibration of the MC simulator against measured characteristics of the 120-nm gate length PHEMT outlining the device structure. The DC simulation results for the scaled devices are detailed in Section 4 while Section 5 deals with an RF analysis of the devices. Conclusions and comments are made in Section 6.

2. The finite element Monte Carlo simulator

A Monte Carlo heterojunction 2D finite element (MC/H2F) device simulator has been developed to study the electron transport properties and the DC and RF characteristics of compound FETs [8,9]. The finite element approach employed in the MC/H2F can reproduce realistically the T-shape gate and the recess region in the device [10]. The MC module includes electron scattering with polar optical phonons; inter- and intra-valley nonpolar optical phonons; acoustic phonons and ionized and neutral impurity scattering. In addition, alloy scattering and strain effects [11] are taken into account in the InGaAs channel. Free surface of the device is assumed to have a constant surface charge of 2×10^{12} cm^{-2} which pins the Fermi level (pinning effect).

The electron scattering rate caused by an alloy potential is calculated using the following formula [12]:

$$\Gamma(E) = \frac{3\pi m^{3/2}}{32\sqrt{2}\hbar^4} a^3 x(1-x)(\mathscr{D}_{\text{alloy}})^2 d\sqrt{E(1+\alpha E)} \times (1+2\alpha E)G(E,E), \quad (1)$$

where x is the fraction of the secondary material; a, the primary material lattice constant; d, the degree of disorder (the order is perfect for $d = 0$ and maximum disorder with $d = 1$) and $\mathscr{D}_{\text{alloy}}$ is the alloy scattering potential. We have taken a theoretically calculated alloy potential [13] which is found to be in very good agreement with experimental data. We set $d = 1$ since the InGaAs channel is 10 nm thick.

In order to extent the validity of the electron transport model to higher electric fields, all scattering rates and generation of final states are modified with a form factor F (the overlap integral) given by [14]

$$F(E,E') = \frac{(1+\alpha E)(1+\alpha' E') + \frac{1}{3}\alpha E \alpha' E'}{(1+2\alpha E)(1+2\alpha' E')}, \quad (2)$$

when an electron with the initial energy E finishes with the final energy E' after a scattering and where α and α' are the non-parabolicity parameters for the electron in initial and final valleys respectively. Note that the nonparabolic energy dispersion is used to represent the band structure and to calculate the scattering rates. Employing the form factor (2) allows us to extend the electric field over which we can confidently predict electron transport properties up to 200 kV/cm.

The analytical band structure model of III–V materials takes into account three valleys: Γ, L and X. Selected material parameters used to simulate bulk transport properties are collected in Table 1. Parameters for ternary alloys have been linearly interpolated between their binary components except for their permittivities and band gaps. Deformation potentials related to the Γ valley were either independently extracted in comparison with experimental v–E characteristics or taken from other work as referred to in Table 1. All other deformation potentials related to L and X valleys and all optical phonon energies have been taken from the full band MC results reported in Ref. [15]. They are not listed in Table 1.

The introduction of these features into the analytical band model for III–V materials requires new calibration procedures which compare simulated bulk drift velocities of the relevant materials against experimental data. The simulated drift velocity as a function of applied electric field shown in Fig. 1 demonstrates that the introduction of the form factor (2) into the scattering rates can substantially improve the agreement with experimental data [18–20] in bulk GaAs at high electric fields up to 200 kV/cm. Likewise, Fig. 2 shows that the simulated drift velocity in bulk $In_{0.53}Ga_{0.47}As$ can follow the trend of the experimental data [21–24] up to the same limit of the electric field. Inclusion of the alloy scattering mechanism decreases the electron drift velocity (shown by plusses in Fig. 2) at low electric fields in the bulk simulation of $In_{0.53}Ga_{0.47}As$. Alloy scattering also plays an important role at very high electric fields where it markedly lowers the carrier velocity. Even with these improvements, the analytical band model is expected to breakdown at very high electric fields (>200 kV/cm) at which point full band models must be considered.

We neglect 2D scattering processes in the device 10-nm thick InGaAs channel. Although 2D electron

Table 1
Selected material parameters used in the MC simulations. Unquoted parameters refer to values determined independently by us

Parameter	Valley	GaAs	AlAs	InAs
Electron effective mass (m_0)	Γ	0.0665[a]	0.149[b]	0.0275
	L	0.222	0.24	0.286
	X	0.58	0.343	0.64
Non-parabolicity factors (1/eV)	Γ	1.16[c]	1.1[c]	2.1093[d]
	L	0.4[c]	0.45[c]	0.45[c]
	X	0.55	0.83[c]	0.9
Acoustic deformation potential (eV)	Γ, L, X	5	7	5.8
Non-polar optical deformation potential ($\times 10^{10}$ eV/m)	L	3.2	3.2	2.0
Non-polar optical phonon energy (meV)	L	34.3	47.5	31.28
Optical deformation potential ($\times 10^{10}$ eV/m)	Γ–L	6.5	10.0	10.0

[a] Ref. [16].
[b] Ref. [17].
[c] Ref. [15].
[d] A non-parabolicity factor in $In_xGa_{1-x}As$ is approximated to the second order.

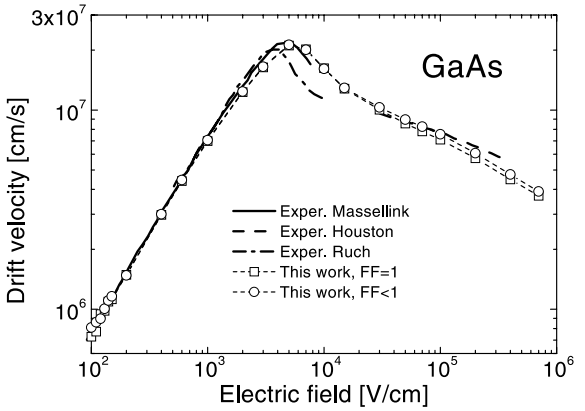

Fig. 1. Drift velocity versus applied electric field in GaAs. Simulated results using the form factor (FF) equal to 1 and less than 1 [14] are compared with experimental data of Refs. [18–20].

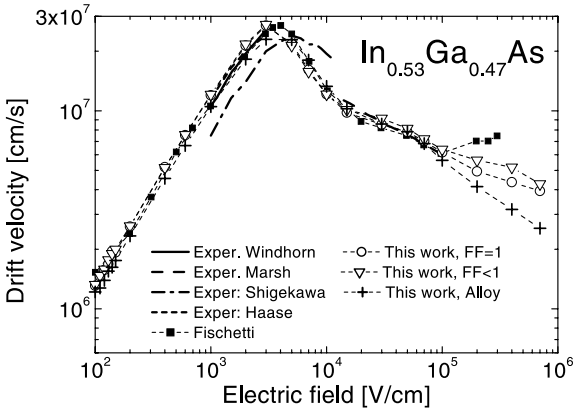

Fig. 2. Drift velocity versus applied electric field in $In_{0.53}Ga_{0.47}As$. Simulated results using the FF equal to 1, by Ref. [14], and including alloy scattering are compared with experimental data of Refs. [21–24] and simulated data of Ref. [15].

transport can increase the drift velocity in III–V materials at low electric fields, at high electric fields, the drift velocity simulated using 2D electron scattering rates in the HEMT channel is very close to the velocity obtained from 3D rates [25]. Intra-sub-band scattering transitions which dominate at low electric fields provide a much faster electron transport than the bulk 3D transport in semiconductors but at high electric fields the probability of inter-sub-band transitions increases dramatically resulting in a transport more akin to the bulk transport. In addition, at high electric fields the electrons start to occupy the higher L and X valleys. The net effect at high electric fields is that an overall drift velocity is very close to the bulk velocity [26]. The whole picture of electron transport in heterostructure can be further complicated by the effect of 2D electron–electron interactions [27] and multi-sub-band screening [26] which can cause further decoherence effects.

3. Calibration procedure

The investigation of PHEMT scaling performance is based on careful calibration of the MC device simulations against a 120-nm gate length PHEMT designed and fabricated in the Nanoelectronics Research Centre at the University of Glasgow. The layout of this device is shown in Fig. 3. It has a T-shaped gate; a 30 nm heavily (4×10^{18} cm^{-3}) Si-doped n+ GaAs cap layer; an $Al_{0.3}Ga_{0.78}As$ etchstop layer; a 7×10^{12} cm^{-2} Si-delta doped layer on top of an $Al_{0.3}Ga_{0.78}As$ spacer layer and, finally, an InGaAs channel with indium content $x = 0.2$.

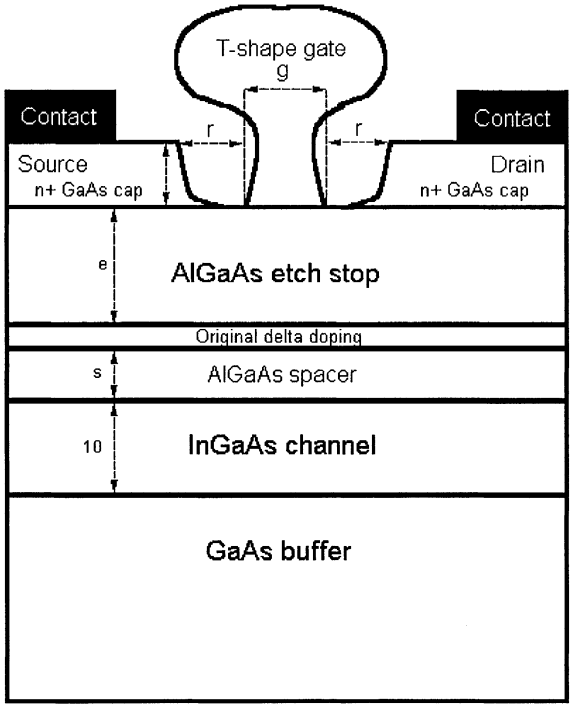

Fig. 3. The cross-section of the simulated PHEMT. All quoted dimensions are in nm and remain unchanged in the scaling process. The distances given by letters (r: recess, e: etchstop and s: spacer) have been scaled according to Table 2.

The whole device structure is grown on top of a 50 nm GaAs buffer.

The measured PHEMT is a two finger device with a total width of 100 μm, embedded in a coplanar waveguide topology compatible with RF, on-wafer probing. All lithographic levels were defined by electron beam lithography using a Leica Cambridge EPBG-5 Beamwriter. The Schottky contact recess trench was produced by selective reactive ion etching in $SiCl_4/SiF_4/O_2$ for 1.2 min to etch the GaAs cap layer, stopping on the 5 nm AlGaAs etchstop layer [28]. The gate metallization of Ti/Pd/Au was deposited on AlGaAs etchstop layer after treated in 4:1 hydrofluoric acid for 60 s.

RF measurements were performed on-wafer in the frequency range 0.24–110 GHz in two steps. 0.24 to 60 GHz using Anritsu-Wiltron VNA with coaxial air-coplanar probes and 67–110 GHz using WR10 air-coplanar probes. GaAs PHEMT devices were measured after Line-reflect–reflect-match calibration [29,30] using 50 Ω NiCr loads on GaAs.

The simulated I–V characteristics obtained directly from the device simulator MC/H2F, represent the typical behaviour of an intrinsic device. To compare this with experimental data contact resistances of the source and drain are included in the I_D–V_D curves at a post-processing stage. The final I_D–V_D characteristics (open symbols in Fig. 4) for gate voltages from −0.6 to 0.4 V are in excellent agreement with the experimental data (full symbols in Fig. 4). The external source resistance, which has been used to remap the intrinsic characteristics according the procedure described in Ref. [31], is 5.22 Ω. This resistance includes 2.4 Ω external to the device, associated with the measurement equipment. For comparison only, a curve corresponding to the intrinsic device at a one gate voltage (0.4 V) is also shown by a dashed line.

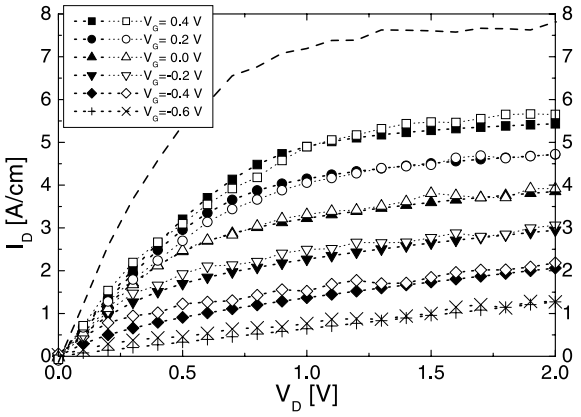

Fig. 4. I–V characteristic (drain current versus drain voltage) of the PHEMT with a gate length of 120 nm. Full symbols represent experimental data for several fixed gate voltages. Open symbols are MC simulations when external resistances of the drain and source are included. The I–V characteristic for an intrinsic device at a gate voltage of 0.4 V (dashed line) is shown for comparison.

4. Effect of scaling on DC PHEMT performance

After calibrating MC/H2F against the existing 120-nm gate length PHEMT, we carry out a simulation study of the scaled devices with gate lengths of 90, 70, 50 and 30 nm using the same material and device parameters. Two possible approaches for the device scaling are compared. The first assumes scaling proportional to the gate length in the lateral dimensions only. The second, referred to as full scaling, assumes that: all lateral dimensions are scaled proportionally, and that the etchstop and spacer are also scaled in the vertical dimensions, to the extent that such scaling is technologically feasible. The thickness of the etchstop and space layers and the extent of the recess considered in the scaling process are collected in Table 2. The 10 nm InGaAs channel and the 30 nm Si-doped cap layer remain unchanged during the scaling process. Note that the devices are assumed to be working at room temperature.

Table 2
Dimensions used in the scaling process as referred to in Fig. 3

	Gate length (nm)				
Dimension of (nm)	120	90	70	50	30
Recess (r)	50	38	29	21	13
Etchstop (e)	18	14	10	7	5
Spacer (s)	7	6	5	4	2

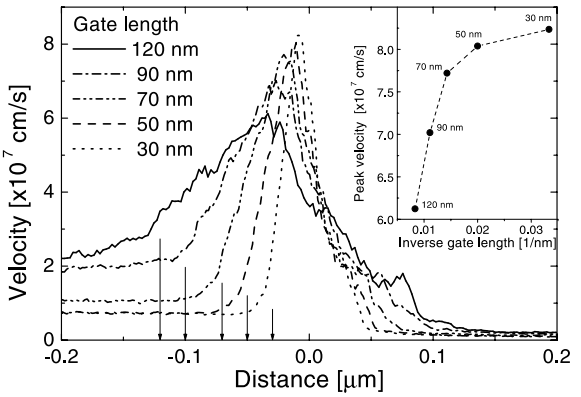

Fig. 5. Average velocity along the InGaAs channel of the scaled PHEMTs for a drain bias of 1.5 V and a gate bias of 0.0 V. The arrows indicate the beginning of a gate for 120, 90, 70, 50 and 30 nm lengths respectively when the gate end is placed at 0.0 μm. The inset shows the peak average velocity versus the inverse gate length.

A rapid increase in the maximum average channel velocity for the fully scaled PHEMTs can be observed in Fig. 5 for gate lengths scaled from 120 to 70 nm at drain and gate biases of 1.5 and 0.0 V respectively. The improvement in channel velocity saturates with the further scaling of the devices to 50 and 30 nm as indicated by the inset of Fig. 5. The continued device improvement despite this velocity saturation results solely from the reduction of the channel length and the decrease in source–drain separation.

When the device gate length reaches deep decanano dimensions it becomes comparable to the inelastic mean-free path of the carriers. Hence, electrons travelling through the gate region have a high probability of passing through this region ballistically (without suffering any collisions). Therefore, the electron transport in the channel beneath the gate has a highly non-equilibrium character leading to a velocity overshoot. Nevertheless, the inset of Fig. 5 shows that the velocity overshoot saturates at smaller gate lengths. A sharp drop in the velocity from its maximum can be observed when electrons reach the extremely high field recess region on the drain side [32] (the drain edge of the gate in Fig. 5 is at 0.0, whilst the arrows are pointing to the

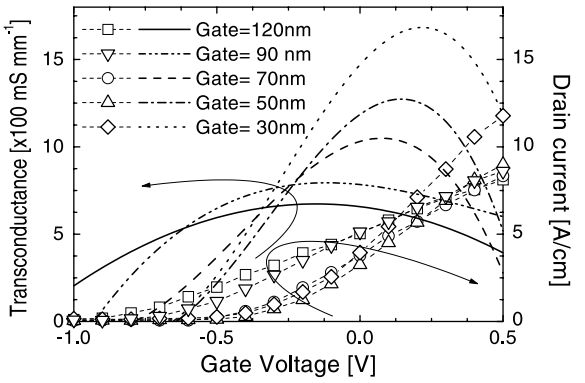

Fig. 6. Transconductance and drain current versus gate voltage for intrinsic devices which are fully scaled at a fixed drain voltage of 1.5 V.

source edge). The velocity drop suggests that an electron which travels ballistically suffers collisions in that region.

The drain current and transconductance of the fully scaled devices are plotted in Fig. 6 as a function of the gate voltage for intrinsic devices at a drain voltage of 1.5 V. The intrinsic transconductance increases steadily during the scaling process, despite the onset of velocity overshoot saturation in the non-equilibrium channel as the gate length is shrunk below 70 nm. However that is not the case for intrinsic devices scaled only in the lateral dimensions. Fig. 7 illustrates the drain current and transconductance in this case as a function of the gate voltage again at $V_D = 1.5$ V. Although the drain current increases when the channel length is reduced, the transconductance starts to decline. This poor behaviour of the laterally only scaled devices is associated with increased drain induced barrier lowering. Therefore, an improvement in PHEMT performance can be only achieved if lateral device scaling is accompanied by a

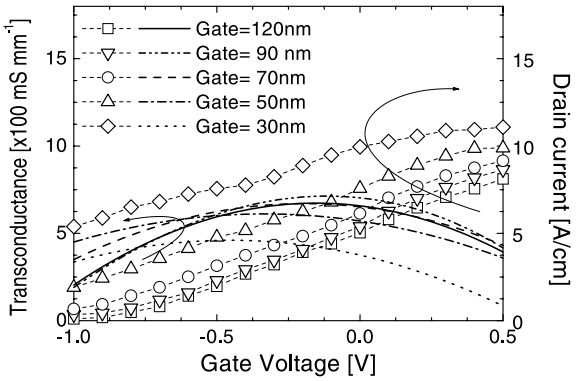

Fig. 7. Transconductance and drain current versus gate voltage for intrinsic devices which are scaled only in the lateral dimensions at $V_D = 1.5$ V.

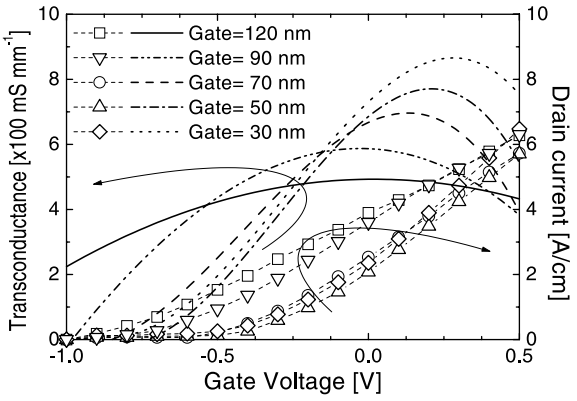

Fig. 8. Transconductance and drain current versus gate voltage with the inclusion of external resistances for fully scaled PHEMTs again at $V_D = 1.5$ V.

similar scaling in the vertical dimension. However, it should be noted that any reduction of the gate to channel separation below 10 nm may require consideration of electron tunnelling between the gate and channel in the simulations. This issue could also cause technological difficulties.

Fig. 8 illustrates the effect of the external contact resistances on the performance of fully scaled PHEMTs, assuming that the value of these resistances remains unchanged in the scaling process. Influence of the external resistances on device performance (both on the drain current and the transconductance) becomes increasingly important with the reduction of the device dimensions. A reduction of contact resistances will be one of the main technological challenges which has to be resolved in order to benefit from the enormous performance potential of scaled intrinsic PHEMTs.

5. RF analysis of the scaled PHEMTs

The computational efficiency and small memory footprint of the MC/H2F compared with full band MC simulation tools permits time domain analysis as a method of modelling the microwave performance of scaled devices. Step voltage changes, usually of 0.2 and 0.3 V respectively, are applied to the gate and then to the drain contacts and the transient responses recorded for a period of 6.0 ps using a modified Ramo-Shockley approach [33]. Although this technique reduces the effects of statistical noise over purely superparticle counting methods, THz oscillations in device drain currents inherent to the MC simulation of devices with heavily doped regions, mask the detailed form of the transients. Up to 100 traces are averaged to define the response, and the magnitude of input voltage step is a compromise between obtaining a response large enough for analysis in the presence of statistical noise, whilst remaining small signal.

On obtaining terminal current responses, complex y-parameters are derived by Fourier analysis. Then the intrinsic cut-off frequency, f_T, can be extracted [34]. To extract the maximum frequency of oscillation, f_{max}, the y-parameters are transformed into s-parameters [34]. After the steady state calibration of the MC simulation to the 120 nm device noted above, extraction of RF results requires no further fitting parameters. However, the simulation model must be augmented by measured source, drain and gate contact resistances if results are to be compared with experimental data. Transformation to z-parameter form allows the addition of external impedances [34].

Fig. 9 shows the sensitivity of f_{max} to parasitic resistances neighbouring those measured for the 120 nm PHEMT, and indicates close agreement with experiment, with an f_{max} of 185 GHz. Assuming external resistances remain unchanged as the device scales to 90 and 70 nm, f_{max} values of 240 and 280 GHz respectively are obtained, whilst intrinsic f_{max} values exceed 1 THz for the 70-nm gate length device. However, continued scaling to 50 and 30 nm devices narrows the transient peak of transconductance to such an extent that step input voltage changes of 0.2 and 0.3 V at the drain and gate cannot be considered small signal and further improvements in RF performance can no longer be distinguished in the MC transients. Increasing statistical noise (due to the reduced proportion of channel superparticles compared to those in the heavily doped cap/contact regions) and the need for smaller step input voltage changes mean that RF simulation of devices smaller than 50-nm gate length is at present computationally prohibitive.

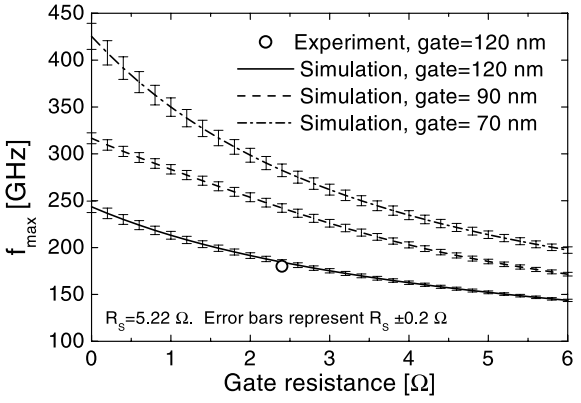

Fig. 9. Maximum frequency of oscillation, f_{max}, as a function of gate, source and drain resistances for PHEMTs with gate lengths of 120, 90, and 70 nm. Open circle shows experimentally measured f_{max} value for the real 120-nm gate length device.

6. Conclusions

Using the MC/H2F, we have studied the performance of PHEMTs with low indium content channels when these devices are scaled to deep decanano dimensions. To increase the confidence in the results the device simulator has been carefully calibrated with respect to a physical PHEMT with a gate length of 120 nm. The average electron channel velocity steadily increases with the scaling to the 70-nm gate length thanks to the non-equilibrium ballistic transport and the resultant velocity overshoot. On further scaling, the velocity saturates due to the increasing effect of backscattering associated with excessively high electric fields in the drain recess region. Despite this we have found a continuous improvement in the intrinsic device performance with proportional scaling. However, in order to take advantage of this performance potential in real devices the contact resistances need to be reduced as far as possible.

Finally, we have performed RF analysis on all the scaled PHEMTs. Remarkable agreement of the MC simulated f_{max} with the experimentally measured value has been obtained. f_{max} exhibits a strong dependence on the parasitic external resistances during the scaling process. A continuous increase of f_{max} has been found when the device gate length is scaled to 90 and 70 nm. But the further scaling to 50 and 30 nm leads to computational difficulties and therefore no f_{max} figures for these channel lengths have been reported.

Acknowledgements

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