Self-aligned 0.12μm T-gate $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ HEMT technology utilising a non-annealed ohmic contact strategy

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Abstract

An InGaAs/InAlAs based HEMT structure lattice matched to an InP substrate is presented in which drive current and transconductance has been optimized through a double-delta doping strategy. Together with an increase in channel carrier density, this allows the use of a non-annealed ohmic contact process. HEMT devices with 120nm standard and self-aligned T-gates were fabricated using the non-annealed ohmic process. At DC self-aligned and standard devices exhibited transconductances of up to 1480 and 1100 mS /mm respectively, while both demonstrated current densities in the range 800 mA/mm. At RF a cutoff frequency f_T of 190GHz was extracted for the self-aligned device. The DC characteristics of the standard devices were then calibrated and modelled using a compound semi-conductor Monte Carlo device simulator. MC simulations provide insight into transport within the channel and illustrate benefits over a single delta doped structure.

1. Introduction

The continuous drive to improve the RF performance of III-V HEMT technology has led to the development of various sub 100nm gate processes [1], and the use of higher indium content based material structures [2]. Such technology finds applications in areas such as high-speed optical-fibre communication systems in addition to high-frequency wireless systems. Shorter gate lengths result in reduced gate - channel capacitances, while increased indium concentrations within the device channel lead to higher carrier concentrations, mobility and velocity, all of which contribute to enhanced device performance. For shorter gate length devices vertical scaling of the material structure is required to maintain effective gate control over channel transport. Unfortunately at shorter gate lengths this scaling has the adverse effect of reducing channel carrier concentration through the reduction of gate to channel separation [3,4]. In addition, parasitic access resistances associated with the source and drain regions are found to dominate over intrinsic device properties at these shorter gate lengths [4,5]. To minimise the negative effect of such parasitics and increase the carrier density within the channel, a double-delta doping strategy can be adopted [6,7]. Further to this, a self-aligned T-gate approach can be incorporated which reduces the separation between the source and drain contacts, further minimising associated access resistances. This process however can lead to difficulties in forming effective low resistance ohmic contacts to the device due to restricted annealing temperatures and ohmic metal heights. Recent research has provided a process for the formation of thin (sub 100nm) non-annealed ohmic contacts to pseudomorphic HEMT (PHEMT) material and allowed the realisation of 120nm self-aligned T-gate PHEMT devices [8]. This idea has been taken further by refining the original PHEMT process and modifying it for compatibility with a lattice matched (lm) InGaAs/InAlAs system. By introducing an additional layer of delta-doping to this structure and modifying the layer dimensions, the source and drain access resistances are reduced by i) maximising vertical conductance through the structure, allowing the use of non-annealed ohmic contacts and hence a self-aligned process, and ii) increasing the overall carrier concentration throughout the structure, reducing parallel resistances.

Self-aligned and standard source-drain separation T-gate lmHEMTs of 120nm gate length were then fabricated using the non-annealed ohmic contact process. Device results indicated excellent values of up to 1480 mS/mm for DC transconductance and an f_T in the range of 190 GHz. In addition the self-aligned devices outperformed those with standard source-drain contact separations considerably at both DC and RF, demonstrating the benefits of the self-aligned process. The benefits of double-delta doping and the non-annealed ohmic process are verified by Monte Carlo (MC) device simulations [3]. The MC device simulations also provide insight into the details of carrier transport in the active regions of the device.

2. Material and Fabrication

Material structure and device dimensions are presented in *Figure 1*. The layer structure is based on a typical lattice matched InGaAs/InAlAs HEMT layout with a highly n^+ doped $In_{0.53}Ga_{0.47}As$ cap followed by an $In_{0.52}Al_{0.48}As$ barrier with selective delta doping. A thin $In_{0.52}Al_{0.48}As$ spacer layer separates the 1st layer of delta doping from the $In_{0.53}Ga_{0.47}As$ channel which is grown upon an $In_{0.52}Al_{0.48}As$ buffer layer and finally an InP substrate. The second layer of delta doping is situated above the first, closer to the cap. The combination of the

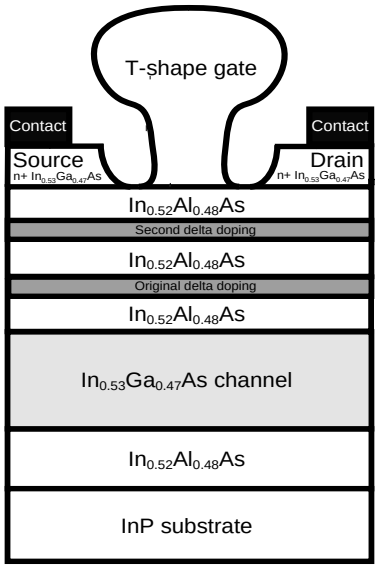

Figure 1 - Cross section of 120 nm gate device and layer structure with double-delta doping

two acts to minimise the impedance of the potential barrier formed between cap and channel regions by the InAlAs layer and hence promote better vertical conduction between the two. It is crucial that the second delta doping layer be properly situated to ensure complete depletion of all layers above the channel upon gate contact formation thus avoiding parallel conduction. The Schottky barrier height must also be sufficiently large to minimise gate leakage. A plot of the conduction band profile and carrier concentration under the gate using a 1D Schroedinger-Poisson solver is presented in *Figure 2*. Van der Pauw measurements of the grown material indicated a capped and capless mobility of 4100 cm^2/Vs and 7100 cm^2/Vs and carrier concentrations of $1.25x10^{13}$ cm^{-2} and $3.35x10^{12}$ cm^{-2} respectively.

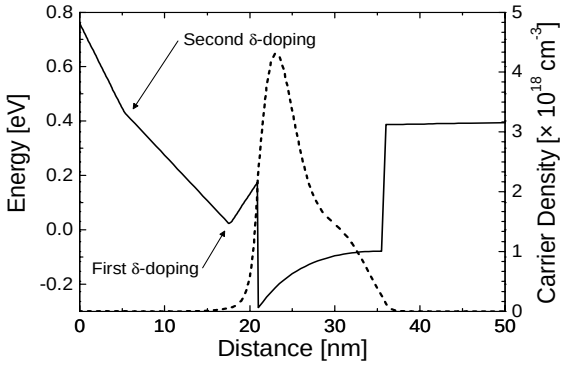

Figure 2 - Conduction band and carrier concentration profiles vs distance under the gate at V_g=0V

Devices with 120nm T-gates were fabricated using the following process:
An orthophosphoric based wet etch was used for mesa isolation, followed by definition of 120nm T-gates using a Leica EBPG5-HR 100 electron beam lithography tool operating at 50keV, with a tri-layer PMMA /P(MMA/MAA) resist stack. A Succinic acid based recess etch was then used to selectively remove the

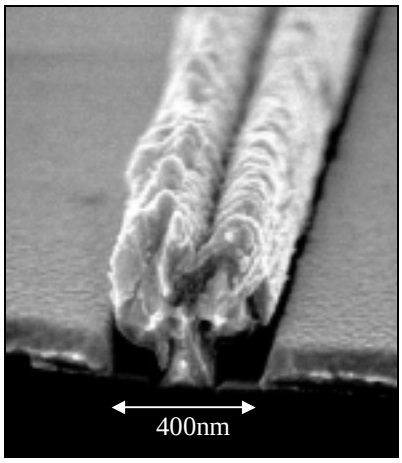

Figure 3 - SEM image of a self-aligned 120nm T-gate.

InGaAs cap, and allow subsequent metalisation of the Ti:Pd:Au gate onto the InAlAs barrier layer. A thin (sub 100nm) Ni:Ge:Au based metalisation was then deposited onto the InGaAs cap to form the non-annealed ohmic contacts. For self-aligned devices, this metalisation was deposited across the gate creating a source-drain contact separation equal to the size of the head of the T-gate, (typically 400nm). For standard devices, the source and drain were formed at a typical separation of 1.6µm. *Figure 3* presents a self-aligned 120nm T-gate structure with a thin ohmic metal deposition forming the source and drain. The discontinuity between ohmic metal and gate head, which is essential to device operation, can be seen clearly along the width of the device. Finally coplanar waveguide bondpads were defined to allow on-wafer DC and RF characterisation. It has been suggested that by keeping the thermal budget of the device process to below 300°C, RF performance can be improved [1]. The use of our non-annealed ohmic contact process meant that thermal processing could be kept to below 180°C.

3. Device Results

Standard source-drain separation and self-aligned devices were characterised at DC using an Agilent 4155 semiconductor parameter analyzer. I_d-V_d characteristics

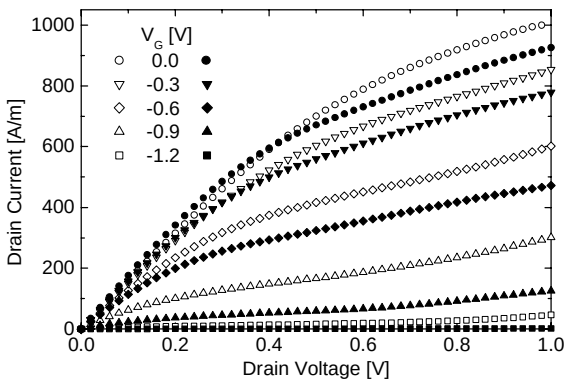

Figure 4 - I_d-V_d comparison for 120nm standard (transparent) and self-aligned devices (opaque)

from both are presented in *Figure 4* for comparison. Reduced access resistance is demonstrated with the self-aligned device at low drain bias where the slope of the I_d-V_d response is steeper than that of the standard device. In contrast the standard device exhibits a higher drain saturation current. This is due to the change in the threshold voltage with the self-aligned devices associated with the proximity of the self-aligned contacts to the gate region. Peak transconductances of 1480 and 1100 mS/mm were recorded for self-aligned and standard devices respectively, with both exhibiting current densities in the range 800 to 900 mA/mm. Transconductance and I_d-V_g curves for both are given in *Figures 5* and *6*.

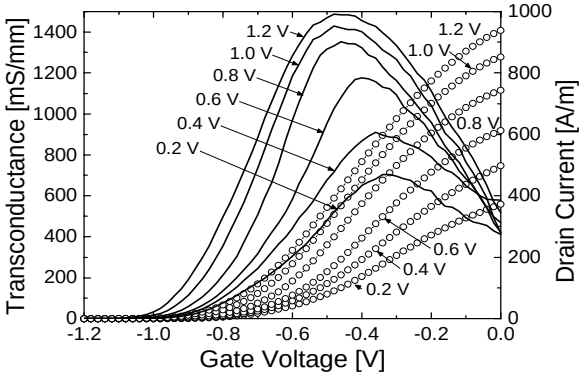

Figure 5 - I_d-V_g (circles) and transconductance (full lines) for a 120nm *self-aligned* device. Drain voltages indicated for each sweep.

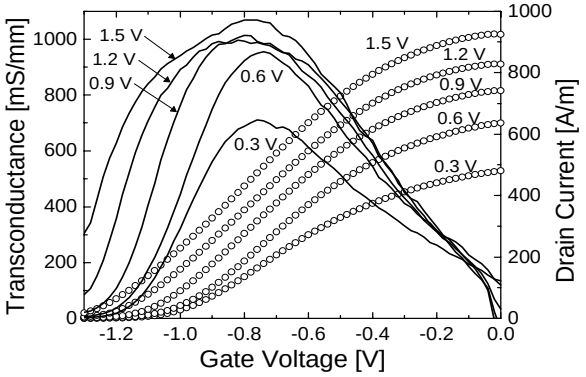

Figure 6 - I_d-V_g (circles) and transconductance (full lines) for a 120nm *standard* device. Drain voltages indicated for each sweep.

By reducing the source access resistance through a self-aligned approach, the transconductance is found to increase substantially, (by over 25%). The gate voltage at which the drain current is 'pinched off' also shifts from -0.9V to –1.2V between self-aligned and standard devices, further demonstrating the reduction in the source resistance.

Multi-bias device s-parameter data was taken using an Anritsu 360B network analyser. This yielded an f_T in the range of 190 GHz for the self-aligned device and 170 GHz for the standard.

4. Monte Carlo Modelling

The MC device simulator, which is employed to model the 120nm lmHEMT has been described in detail elsewhere [3]. The MC module includes electron scattering with polar optical phonons, inter- and intra-valley non-polar optical phonons, acoustic phonons, ionized and neutral impurity scattering, and alloy potential scattering within the non-parabolic dispersion approximation.

All scattering rates and the generation of the final states are calculated using a form factor less than one in order to extend the validity of the transport model up to 400 kV/cm [3]. Both active concentrations of the delta doping layers have been calibrated with the self-consistent Poisson-Schrödinger solver against the experimentally obtained sheet density in the device. The 1st and 2nd delta doping layers are assumed to have active doping concentrations of 4.0×10^{12} cm^{-2} and 2.0×10^{12} cm^{-2} respectively, giving a similar measured sheet density of 3.344×10^{12} cm^{-2}.

The MC device simulation represents an intrinsic device. To allow direct comparison between simulated and experimental data, external contact resistances have to be included [9].

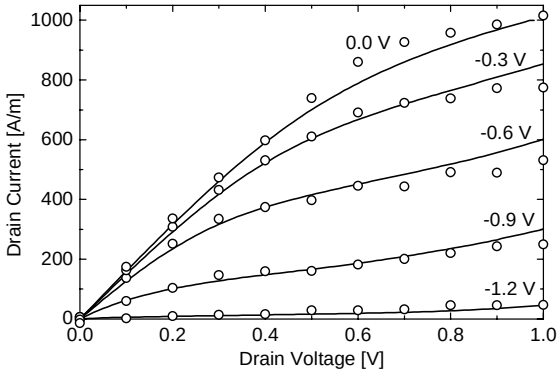

Figure 7 - Calibration of I_d-V_d characteristics obtained from MC device simulations (circles) against experimental data (full lines) for a standard 120nm device. Gate voltages are indicated for each sweep.

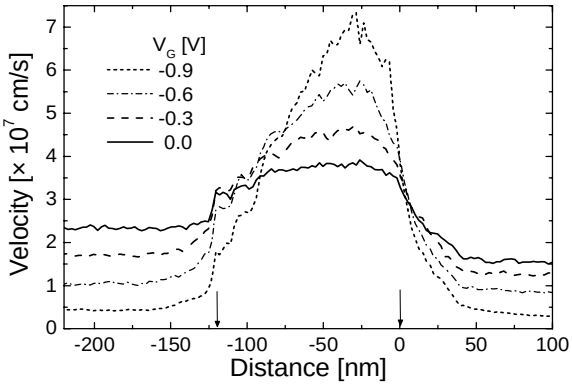

Figure 8 - Average velocity along the channel for a standard 120nm device at V_d = 1.0V. Gate voltages as indicated. The gate region is marked by arrows.

Figure 7 shows excellent agreement between the re-mapped I_d-V_d characteristics obtained from MC simulations and experimental data at gate voltages fixed at –1.2V to 0V with a 0.3V step. The external source and drain resistances used in *Figure 7* to calibrate intrinsic simulations were 1.1 and 0.9 Ω respectively. These low values were in good agreement with experimental data.
Figure 8 shows average electron velocities along the channel for a standard 120nm device. The peak velocity at the drain end of the channel steadily decreases with increasing gate voltage but the velocity near the source increases. The ballisticity of the electron transport below the gate is also reduced at high gate voltages. As illustrated in *Figure 9*, the double doped device delivers higher drain current compared to the single doped one mainly due to increased channel carrier concentration.

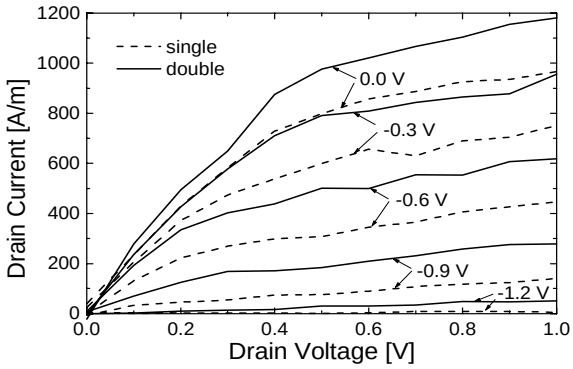

Figure 9 - Intrinsic I_d-V_d characteristics for a standard double-delta doped 120nm device compared with those for a single doped 120nm device. Both results were attained from calibrated MC device simulations.

5. Discussion and Conclusions

We have developed a viable non-annealed ohmic contact process for an InGaAs/InAlAs HEMT material system utilising a double-delta doping strategy. The benefits of a self-aligned gate process have been demonstrated through comparison with those with standard source-drain separation. In addition, MC simulations of the standard device has demonstrated that even though the average velocity below the gate is smaller than for a single doped device, higher current densities arise from a larger channel carrier density. It has been proposed that the reduction of parasitic access resistances and the increase of channel carrier densities will be mostly beneficial to proportionally scaled shorter gate length (sub 100nm) HEMT devices [3,5]. Research is therefore undergoing into the merging of the presented self-aligned technology with existing sub 100nm gate length processes to yield maximum device performance at reduced gate lengths.

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