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Current variations in pHEMTs introduced by channel composition fluctuations

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Abstract. We have studied the impact of the channel composition fluctuations in pseudomorphic high electron mobility transistors (PHEMTs) on the device characteristics. The simulations are carried out using a 3D parallel finite element device simulator based on the drift-diffusion approximation to the semiconductor transport. The variation of the drain current introduced by the channel composition fluctuations increase with the increase of the gate and the drain voltage.

1. Introduction

High performance figures of merit have been reported [1] for high electron mobility transistors (HEMTs) utilising AlGaAs/InGaAs and InAlAs/InGaAs vertical layer structures. However, their performance and reliability can be affected by fluctuations in the ternary alloy composition of the InGaAs channel and the discrete random dopants in the delta doping layer, specially when these devices are scaled to deep sub-micron dimensions [2]. To account for these effects, 3D simulations which capture the full geometry of the device has to be employed. In addition, the study of the random composition variations and the corresponding material properties variations requires the statistical simulation of an ensemble of devices. Such simulations are computational costly and could benefit from the use of parallel algorithms.

In this work we study the influence of random fluctuations in the Indium content of the $In_{0.2}Ga_{0.8}As$ channel in a 120 nm gate length pseudomorphic HEMT (PHEMT). The simulations are carried out with a 3D heterojunction device simulator based on the drift-diffusion (D-D) approach utilising finite element discretisation on an unstructured tetrahedral mesh [3]. In order to reduce the computational time necessary for statistical studies the simulator has been fully parallelised via the Message Passing Interface (MPI) standard library [4].

The paper is organized as follows. Section 2 describes the essential characteristics of the 3D parallel D-D simulator. The basic structure of the simulated device is presented in Section 3 which also introduces the basics of the intrinsic parameter fluctuations in the D-D context and presents the main numerical results. Conclusions and comments are drawn in Section 4.

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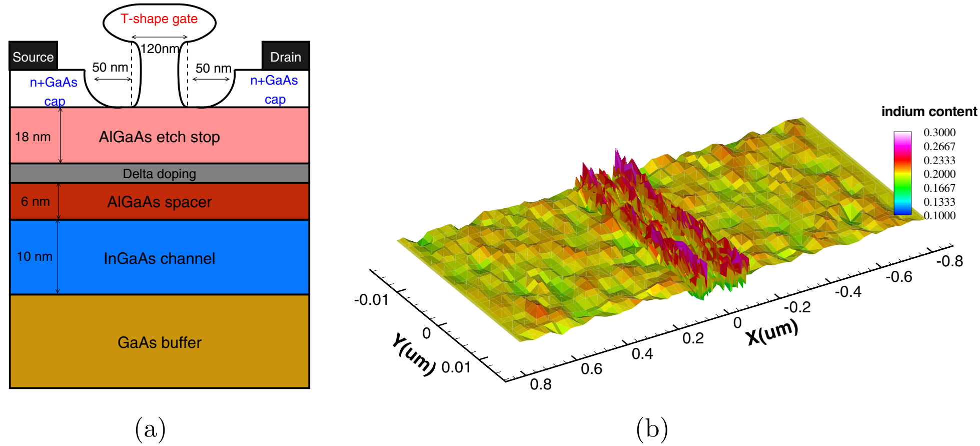

Figure 1. (a) Cross-section diagram of the 120 nm PHEMT and (b) example of a random Indium content distribution inside the $In_{0.2}Ga_{0.8}As$ channel.

2. The Simulation Approach

In our 3D simulator the Poisson equation and the electron continuity equation are discretised using the finite element method. The solution domain representing the simulated device is triangulated using tetrahedrons with the QMG program [5]. The mesh generator, which is based on the octree algorithm, produces an unstructured mesh. The smallest tetrahedra were used below the gate and in the recess regions of the device in order to reproduce accurately the large gradients of the potential and the electron concentrations. Then the METIS program [6] is used to partition the mesh into subdomains distributed and solved in parallel on a distributed memory multiprocessor system. This program has also been used to achieve an improved ordering of the nodes of each subdomain.

3. Results and Discussion

A schematic cross-section of the 120 nm gate length PHEMT with a 30 nm heavily Si-doped (4×10^{18}cm^{-3}) n^+GaAs cap layer, an 18 nm $Al_{0.3}Ga_{0.7}As$ etch stop layer, and a 3.5x10^{12}cm^{-2} Si delta doping layer on top of an 6 nm $Al_{0.3}Ga_{0.7}As$ spacer which separates the delta doping from a 10 nm $In_{0.2}Ga_{0.8}As$ channel is shown in Fig. 1(a). The whole vertical device structure is grown on top of a 50 nm GaAs buffer.

In the simulation, a field dependent mobility model [9] has been employed. This model includes as material parameters the low field mobility and the saturation velocity. We have used a low field mobility of 3800 cm^2/Vs and saturation velocity of 2.5×10^7 cm/s for the $In_{0.2}Ga_{0.8}As$ channel, and of 3000 cm^2/Vs and 1.0×10^7 cm/s for the $Al_{0.3}Ga_{0.7}As$ layers. The high saturation velocity in the channel mimics in the drift-diffusion simulations the velocity overshoot effects.

The study of intrinsic parameter fluctuations is based on careful calibration of the I_D-V_G characteristics against experimental data obtained from a 120 nm gate length pseudomorphic HEMT, designed and fabricated in the Nanoelectronics Research Centre at the University of Glasgow, as well as against the data obtained from a Monte Carlo (MC) device simulator H2F/MC [10] which has been used to deduce the value of the saturation velocity in the channel.

In order to realistically generate the channel composition fluctuations, a 3D crystal lattice was used with the same dimensions as the channel. The position of the In, Ga and As atoms in the crystal lattice have been randomly generated according to the channel composition. Each node of the lattice mesh in the corresponding condensation domain has then been assigned to the nearest node of the tetrahedral mesh creating a random distribution of Indium content inside the channel which varies from 0.1 up to 0.3. This is used to update physical parameters of D-D

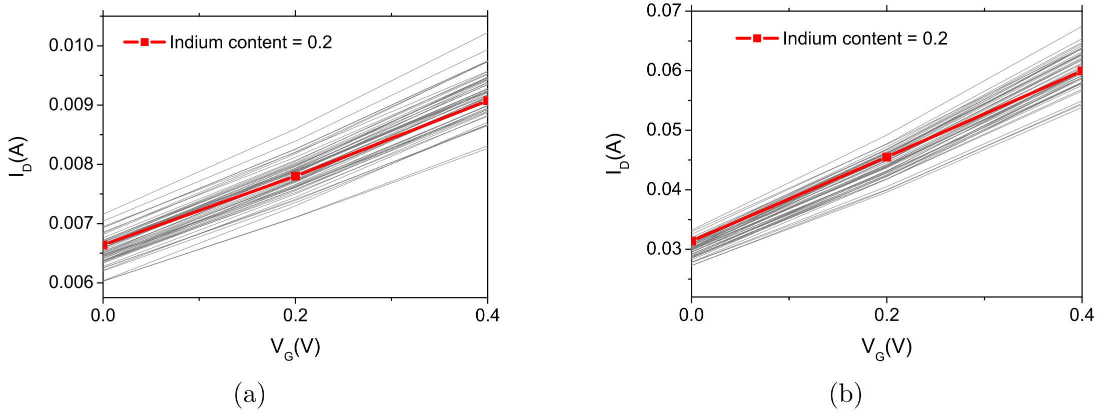

Figure 2. I_D-V_G characteristics at drain biases of 0.1 V (a) and 1.0 V (b) for different random Indium content distributions in the channel of a 120 nm PHEMT.

model such as the mobility, the dielectric constant and the energy bandgap. An internal cross-section view of a particular random Indium content distribution along the channel is shown in Fig. 1(b). The large variations in Indium content found below the gate and recesses is associated with the small size of the elements in these regions.

characteristics at a low drain bias of 0.1 V and at a high drain bias of 1.0 V for different random Indium content distributions (50 configurations) are shown in Figs. 2(a) and 2(b), respectively. The results obtained using uniform Indium content of 0.2 are also included for a comparison. Fluctuations in the indium content have a greater influence on the device characteristics at a high drain current of 1.0 V than at a lower current observed of 0.1 V. This observation is supported by Table 1 where statistical parameters, namely the mean value of the drain current, the normalized standard deviation in the drain current ($\sigma I_D/I_D$), the skewness and the kurtosis, characterising the nature of the obtained distributions, are collected. The normalized standard deviation for the drain current at $V_D = 1.0$ V is always larger than the respective standard deviation for the drain current at $V_D = 0.1$ V. When the drain bias is increased, the electric field is higher, leading to more pronounced variations in the mobility, which are the main contribution to the current variation. Results also show an increase of the fluctuations with the increase of the applied gate voltage. The averaged drain current associated with Indium content fluctuations is in general lower than the current obtained using a constant indium content of 0.2 apart from at $V_G = 0.4$ V where we have found the opposite behaviour.

We have also investigated the effect of the channel width on the standard deviation in the drain current. Therefore, we have varied the width of the channel from 30 to 60 and 120 nm. Fig. 3, illustrates the channel width dependence of the normalized standard deviation in the drain current at low drain bias of 0.1 V and at high drain bias of 1.0 V, showing a decrease of the standard deviation with the increase in the channel width.

4. Conclusions

Using a 3D parallel D-D device simulator we have investigated the influence of random indium content fluctuations inside the $In_{0.2}Ga_{0.8}As$ channel of a 120 nm PHEMT. To increase the confidence in these results the device simulator has been carefully calibrated against the measured characteristics of real 120 nm gate length PHEMT and results from the MC simulation of the same device. The current variations due to indium content fluctuations in the channel of

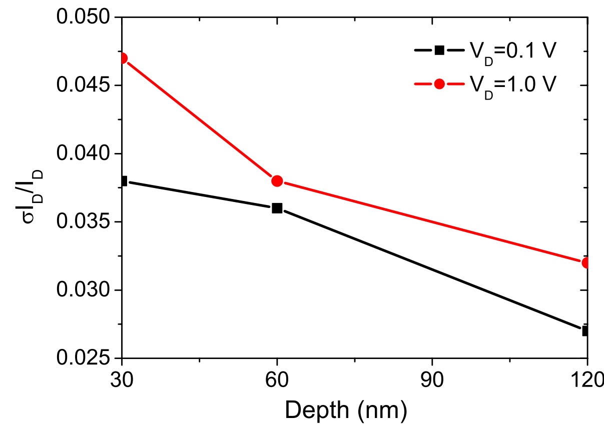

Figure 3. Normalized standard deviation in the current as a function of the depth of the device, calculated at low drain voltage of 0.1 V and at high drain voltage of 1.0 V.

the device increase with the increase of the gate bias, and are also more pronounced at high drain voltage. The normalized standard deviation in the drain current decreases with the increase of the channel width of the transistor.

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Table 1. Statistical parameters characterising the random Indium content distributions at $V_D =$ 0.1 V and $V_D =$ 1.0 V.

	$V_G(V)$	$I_{D,0.2}(mA)$	$I_{D,mean}(mA)$	$\sigma I_D/I_D$	$Kurtosis$	$Skew$
V_D=0.1 V	0.0	6.638	6.547	0.037	0.208	0.029
	0.2	7.799	7.803	0.038	0.460	-0.014
	0.4	9.075	9.205	0.040	0.718	-0.049
V_D=1.0 V	0.0	31.387	29.948	0.047	-0.297	0.147
	0.2	45.488	44.182	0.050	-0.438	-0.101
	0.4	59.975	60.212	0.062	3.863	-1.267